Master thesis : Fast and Flexible Decision Making using CMOS Hardware

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Fast and Flexible Decision Making using CMOS Hardware

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Summary

This thesis focuses on the study and implementation of neuromorphic circuits capable of demonstrating multistability and hysteresis, inspired by biological neural processes. The main objective is to design a hardware system that mimics fast and flexible decision-making behavior. The work begins with an introduction to CMOS transistors, the circuits used and their operation. This is followed by a detailed study of bifurcations, feedback loops and the mathematical principles that lead to the existence of several equilibria. Possible equilibrium changes are explored and supported by numerical simulations performed in Julia. These principles are then implemented in an electrical circuit using the Cadence Virtuoso tool. The different simulations demonstrate the behavior of bistable and tristable circuits, with a particular focus on hysteresis loops that highlight state-dependent transitions and region of multistability. Experimental results confirmed theoretical predictions, showing multistable behavior with equilibrium states dependent on initial conditions and input current. This demonstrates the potential of CMOS neuromorphic circuits for low-power, biologically inspired decision-making. In conclusion, the combination of theoretical modeling, circuit simulations, and experimental testing validates the approach and provides insights into the design of energy-efficient and adaptive neuromorphic systems.

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Chapter 1

Introduction

1.1 Background Information

Biological brains surpass modern hardware and software in solving complex problems with unparalleled energy efficiency. Human and simpler animal neural systems exhibit remarkable adaptability, robustness, and competence, especially when compared to artificial systems in terms of energy consumption. This disparity highlights the limitations of conventional computing architectures and motivates the development of biologically inspired approaches [1].

The brain's efficiency stems from its unique computational architecture. Unlike traditional computers that rely on centralized and sequential processing, the brain operates as a distributed network of billions of neurons. These neurons communicate asynchronously through adaptable connections known as synapses, integrating information processing and memory. Signals are dynamically transformed by the dendritic and axonal structures of neurons, enabling localized interactions that collectively produce the global functionality that drives our everyday functioning. This distributed, adaptive organization guarantees seamless processing of external stimuli, even in the face of variability and uncertainty [1],[2],[3].

A cornerstone of the brain's adaptability is the principle of feedback [4], [5], [6], which regulates neural dynamics and learning. Feedback mechanisms modulate neuronal activity by amplifying or suppressing signals based on specific inputs, ensuring stability and adaptability in complex systems. Synaptic plasticity defines the ability of synaptic connections to strengthen or weaken in response to a particular event, reinforcing the brain's capacity for learning and memory.

Another important phenomenon observed in the brain is hysteresis, which refers to the system's dependence on previous states rather than solely on current inputs. In the brain, hysteresis plays an essential role in processes such as sensory perception, decision-making and memory. It enables neurons to maintain persistent activity or "memory states" even when external stimuli change or disappear. This enables the brain to present robust, context-dependent responses while maintaining smooth transitions between states. For example, hysteresis in motor control circuits enables stable execution of movements despite variable sensory inputs, as shown in the article by [7].

These principles of modulation, adaptation, and self-organization form the basis for designing artificial systems that emulate intelligent behavior [1].

1.2 Problem Statement

Positive feedback mechanisms are pivotal in modeling systems with multiple equilibrium states and hysteresis, as extensively studied in [5], [6]. However, reproducing these dynamics in neuromorphic circuits using CMOS transistors presents unique challenges. This thesis addresses these challenges by reproducing such behaviors while taking into account the inherent constraints of transistor-based systems. In addition, we will try to achieve richer dynamics by having behaviors with more than 2 stable states. Neuromorphic circuits offer low power consumption, making them ideally suited to the reproduction of these complex biological behaviors.[3].

1.3 Methodology

The primary objective of this thesis is to design and implement circuits capable of demonstrating multistability and hysteresis. This work explores these phenomena in depth, examining their significance and potential applications in neuromorphic circuit design. The thesis is organized into three main parts:

1. **Chapter 2**: Introduction of CMOS transitors and their use in neuromorphic circuits. Two electrical circuits using CMOS transitors will be presented and their theoretical behavior will be explored. The circuits presented will serve as a basis for the remainder of the work.

2. **Chapters 3 and 4**: Theoretical background and analysis of non-linear system, feedback, bifurcation and hysteresis, supported by simulations performed in *Julia*. These simulations validate and illustrate the theoretical concepts.

3. **Chapters 5 and 6**: The implementation of these phenomena in circuits, bridging the gap between theoretical principles and practical application. These chapters bridge the gap between the previous chapters.

An important aspect of this project was mastering the *Cadence Virtuoso* platform, a state-of-the-art tool widely used in the semiconductor industry for analog and digital circuit design. In addition to learning the software, the focus was on the design and simulation of neuromorphic circuits to demonstrate the feasibility of theoretical principles in real-world applications. The circuits were developed using the *General Purpose Development Kit 180* (GPDK180), which supports transistor models with a minimum size of 180 nm. In addition, the *analogLib* library provided essential components for simulating sub-threshold and current-mode circuits.

By combining theoretical analysis and practical circuit design this work underscores the potential of multistability and hysteresis to advance low-power neuromorphic systems.

Chapter 2

Neuromorphic CMOS Hardware

2.1 MOSFETs in Neuromorphic Architecture Design

Neuromorphic engineering, inspired by the nervous system, seeks to translate these principles into artificial neural systems. Implementing these systems may involve using CMOS (complementary metal-oxide-semiconductor) technology to emulate the behavior of neurons and synapses. CMOS circuits provide a versatile platform for reproducing biologically-inspired dynamics, including feedback interactions and signal modulation. By taking advantage of the non-linear properties of CMOS technology, neuromorphic systems can achieve functionalities that are efficient and adaptable to changing conditions[8], [9].

CMOS (Complementary Metal-Oxide-Semiconductor) technology is based on two types of transistor: NMOS (n-type MOSFET) and PMOS (p-type MOSFET). These two types of transistor are essential for CMOS circuits, as they work in complementary ways. Understanding their differences and how they work is essential for designing efficient circuits, especially in neuromorphic systems. Here is a brief explanation of the differences between NMOS and PMOS Transistors :

- **NMOS Transistors:** NMOS transistors use electrons as charge carriers. They are activated when a positive voltage is applied to the gate terminal, allowing current to flow between the drain and source terminals. In the case of NMOS, the source voltage is at the lowest potential and the drain voltage at the highest potential. This is due to the fact that electrons are negative charges. NMOS transistors generally have higher mobility due to the faster movement of electrons

compared to holes, making them more efficient for certain operations.

- **PMOS Transistors:** PMOS transistors use holes as charge carriers. They are activated when a negative voltage is applied to the gate terminal, allowing current to flow from source to drain. In the case of PMOS transistors, the source voltage is at the highest potential and the drain voltage at the lowest. This is because holes are positive charges. PMOS transistors are generally slower than NMOS transistors, due to the lower mobility of the holes. However, they consume less power when inactive, as they do not have as high off-state leakage currents as NMOS transistors see Figure 2.2.

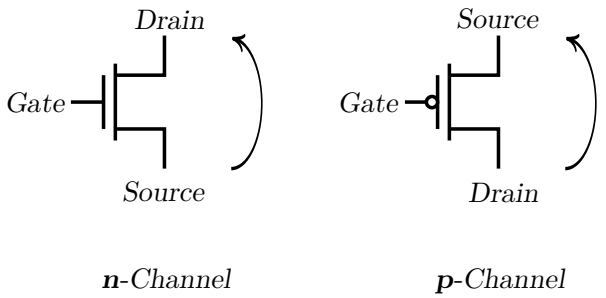


Figure 2.1: Circuit symbols for NMOS and PMOS transistors. Note that the assignment of the source and drain terminals depends on the voltages applied to them, as the physical structure is symmetrical. The arrow indicates the direction of positive potential.

CMOS transistors can operate in two main regimes: above threshold and below threshold. Whereas conventional circuits generally use the above-threshold regime for digital operations [10]. In these cicruits, the sub-threshold region is considered a leakage current region and is treated as an undesirable effect in the circuit. In contrast, the approach of [3], which deals with neuromorphic circuits, exploits the sub-threshold regime because of its unique characteristics, which align with the analog, low-power nature of biological systems.

In the subthreshold region the transistor operates below its threshold voltage (V_{th}). In this regime, the current through the MOSFET follows an exponential dependence on the gate-source voltage (V_{gs}), and is described by the following equations :

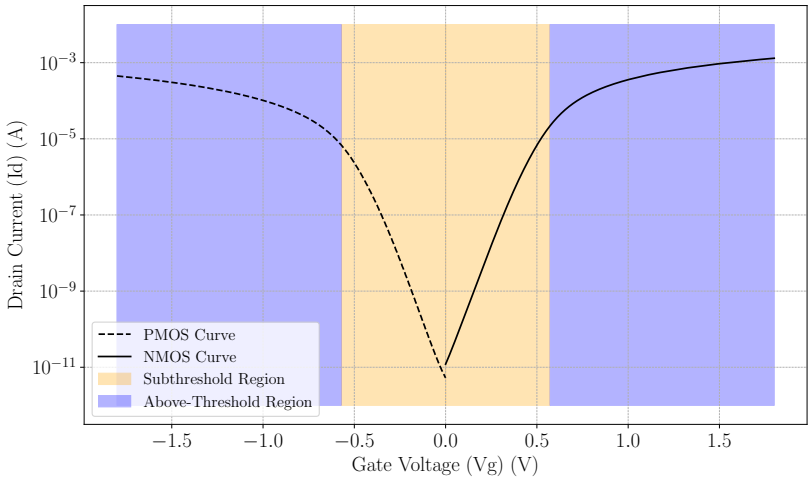


Figure 2.2: MOSFET characteristic I-V. Simulation results obtained using *Cadence* with the *gpdk180* transistor model. PMOS: $L = 300\,\text{nm}$, $W = 3.5\,\mu\text{m}$. NMOS: $L = 300\,\text{nm}$, $W = 3\,\mu\text{m}$. $V_{dd} = 1.8\,\text{V}$. The current on the y-axis is shown on a logarithmic scale to highlight behavior in the subthreshold region.

$$\text{NMOS characteristics: } I_{d\to s} = I_{n0} e^{\kappa_n \frac{V_g}{U_T}} \left(e^{-\frac{V_s}{U_T}} - e^{-\frac{V_d}{U_T}} \right). \tag{2.1}$$

$$\text{PMOS characteristics: } I_{d\to s} = I_{p0} e^{\kappa_p \frac{V_{dd}-V_g}{U_T}} \left(e^{-\frac{V_{dd}-V_s}{U_T}} - e^{-\frac{V_{dd}-V_d}{U_T}} \right). \tag{2.2}$$

Where :

- $I_{n0/p0}$ denote the NMOS/PMOS current scaling parameter (reference current).
- $\kappa_{n/p}$ denote the NMOS/PMOS subthreshold slope factor, a dimensionless parameter that depends on the transistor technology.
- U_T is the thermal voltage, approximately 26 mV at room temperature.
- V_g is the gate voltage, V_s is the source voltage, V_d is the drain voltage.
- V_{dd} is the supply voltage.

In the remainder of this work, we will assume that $\kappa_n = \kappa_p = \kappa$ and $I_{n0} = I_{p0} = I_0$. Now that we've introduced CMOS components and how they work, we can present the circuits we'll be using. All circuits are used in current mode. The equations presented consider Early's effect to be ignored.

2.2 Differential Pair Integrator

The differential pair integrator (DPI) is a key component of neuromorphic circuits, mimicking the temporal dynamics of biological synapses by acting as a logarithmic temporal filter. It converts the input current into a logarithmic voltage, linearly integrates it, then reconverts the filtered signal into current, while guaranteeing wide dynamic range and low power consumption.

The DPI circuit is shown in Figure 2.3. In practice, the current I_τ is imposed by a current mirror. One might ask why not use a current source to control I_τ. The main reason is that the current mirror provides better stability and helps prevent undesirable behaviors. For instance, when V_c gets close to 0 V, a conventional current source could cause the load to reverse, which would disrupt the operation of the DPI circuit. On the schematic, only V_τ is shown for readability.

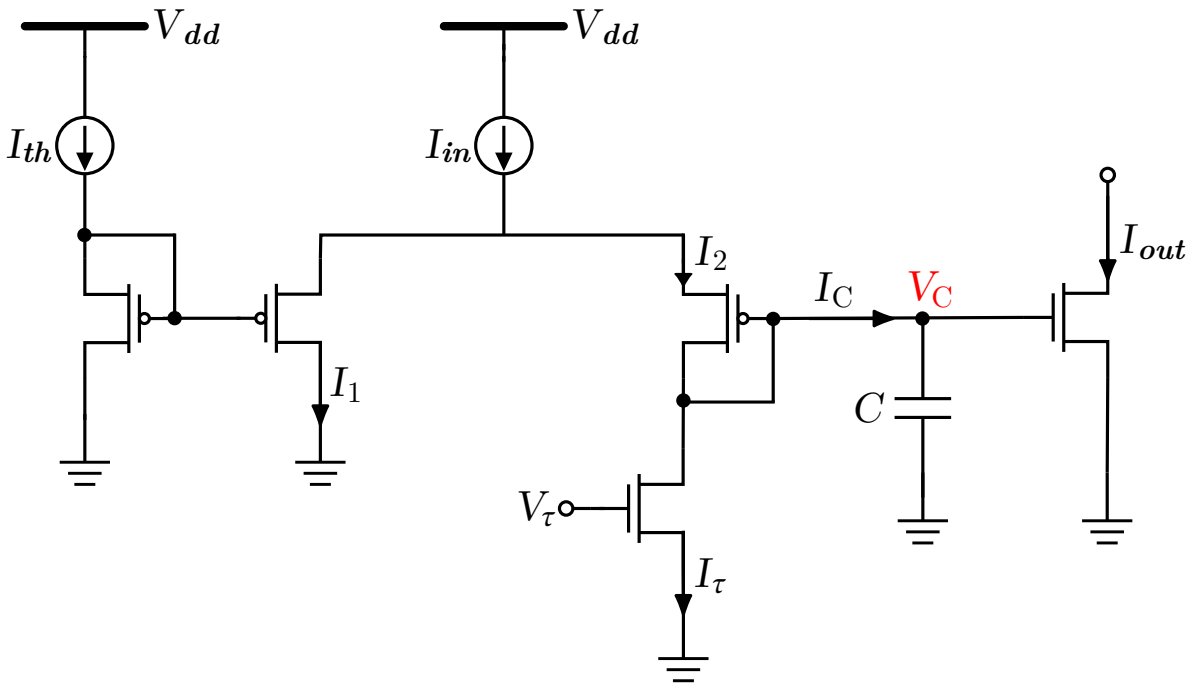


Figure 2.3: Schematic of the Differential Pair Integrator (DPI) circuit.

2.2.1 Equations

To understand the circuit behavior of the DPI in current mode, we start with the fundamental translinear principle [11]:

$$I_{th} I_1 = I_2 I_{out}. \tag{2.3}$$

From the circuit, we can derive the following equations:

$$\begin{aligned} I_2 &= I_\tau + I_C, \\ I_1 &= I_{in} - I_2, \\ \frac{dI_{out}}{dt} &= I_{out} \frac{\kappa}{U_T} \frac{dV_C}{dt}, \\ I_C &= C \frac{dV_C}{dt}. \end{aligned} \tag{2.4}$$

By combining these equations and assuming $I_{in} \gg I_\tau$ and $G = \frac{I_{th}}{I_\tau}$, we derive:

$$\tau \dot{I}_{out} = -I_{out} + G I_{in}, \tag{2.5}$$

where the time constant τ is given by:

$$\tau = \frac{C U_T}{\kappa I_\tau}. \tag{2.6}$$

2.2.2 Behavior

The derived differential equation describes the behavior of the output current with respect to the input current. This equation shows that the DPI acts as an integrator with a time constant τ. If we analyze the system's frequency response using the Laplce transformation, we see that the system behaves like a first order low-pass filter:

$$H(s) = \frac{I_{out}}{I_{in}} = \frac{G}{(\tau s + 1)}. \tag{2.7}$$

Figure 2.4 illustrates the expected behavior of the DPI circuit. The Bode diagram with a gain of 1 (Figure 2.4c) confirms that the DPI functions as a low-pass filter. The diagram shows a cutoff frequency corresponding to $f_c = \frac{1}{2\pi\tau} = 4.28\,\text{Hz}$. Graphically, this cutoff frequency is identified as the point where the gain drops by -3 dB. The Bode plot also demonstrates the characteristics of a first-order low-pass filter, with a 90-degree phase shift and a gain slope of -20 dB per decade beyond the cutoff frequency.

Additionally, Figures 2.4a and 2.4b, which present the response of the DPI circuit to a rectangular input, further illustrate the low-pass filtering behavior and highlight the impact of the gain and the time constant on the system's performance. The input signal is a rectangular pulse with an amplitude of 100 nA, a high pulse duration of 200 ms, and a low pulse duration of 300 ms. This ensures that the signal has sufficient time to return to baseline, and avoids situations similar to when τ is too large, as seen in Figure 2.4b.

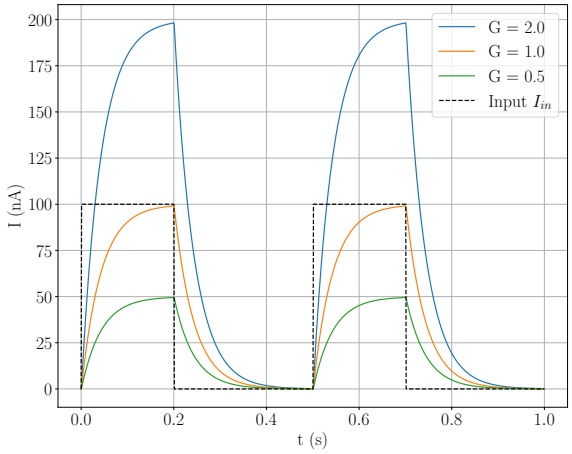
The gain scales the amplitude of the output signal, while the time constant determines the system's reaction time to variations in the input signal. For example, when the gain is too large, the system cannot fully reach the high value of the input signal, and cannot fully return to the low value (see Figure 2.4b), which shows the importance of carefully selecting these parameters according to the requirements of the application.

In practice, the threshold current I_{th} is set as $I_{th} = G \cdot I_{\tau}$, meaning the circuit's behavior can be adjusted by modifying I_{τ}, G, and C. In our experiments, we varied the time constant by using three different values for the DPI's capacitor. As a reminder, the capacitor directly influences the time constant, as described in Equation 2.6.

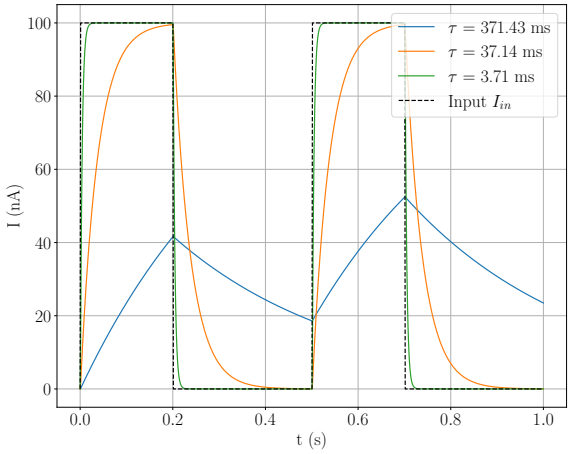
2.2.3 Parameters

Each parameter in the DPI circuit plays a specific role:

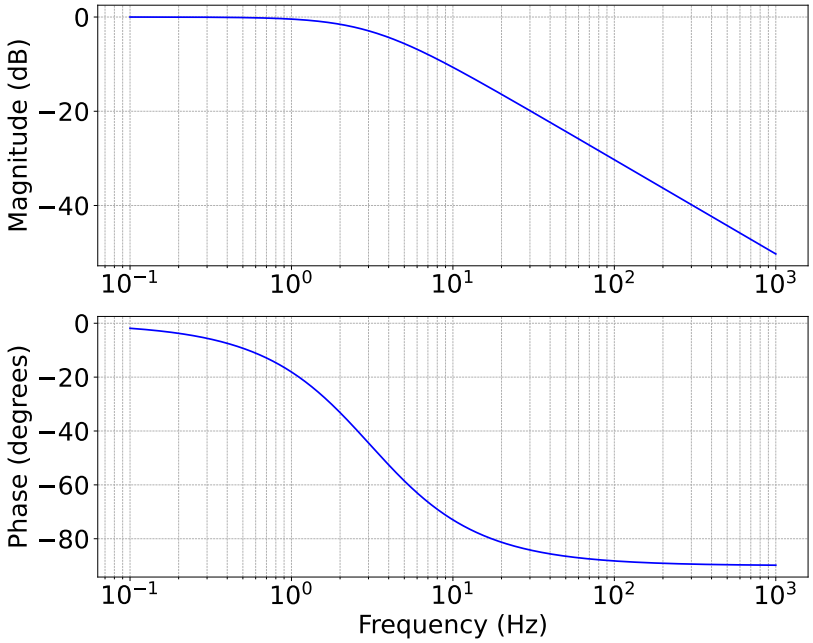
- I_{th}: Threshold current, a scaling factor derived from the translinear principle, which has an impact on circuit behavior and, more specifically, on gain.
- I_{τ}: A current that contributes to the τ time constant. I_{th} and I_{tau} must be of similar magnitudes to maintain stable circuit behavior and to have consistent gain values. Both currents must be relatively low to avoid excessive power consumption and ensure correct integration.
- C: capacitor, which stores charge and influences the time constant τ.



(a) DPI input/output response for $G = 1$, $G = 2$, and $G = 0.5$ with $C = 70$ pF.



(b) DPI input/output response for $C = 7$ pF, $C = 70$ pF and $C = 700$ pF with $G = 1$.



(c) Bode diagram of the DPI for $G = 1$ and $C = 70$ pF, illustrating the theoretical frequency response.

Figure 2.4: Simulated behavior of the DPI using *Julia*, with all simulations assuming $I_\tau = 70$ pF. The transient response is simulated with a rectangular input signal with an amplitude of 100 nA and a duty cycle of 40%.

2.3 Sigmoid Circuit

In this section, we present the design and behavior of the sigmoid circuit [12]. This circuit allows us to incorporate non-linearity into our circuit design.

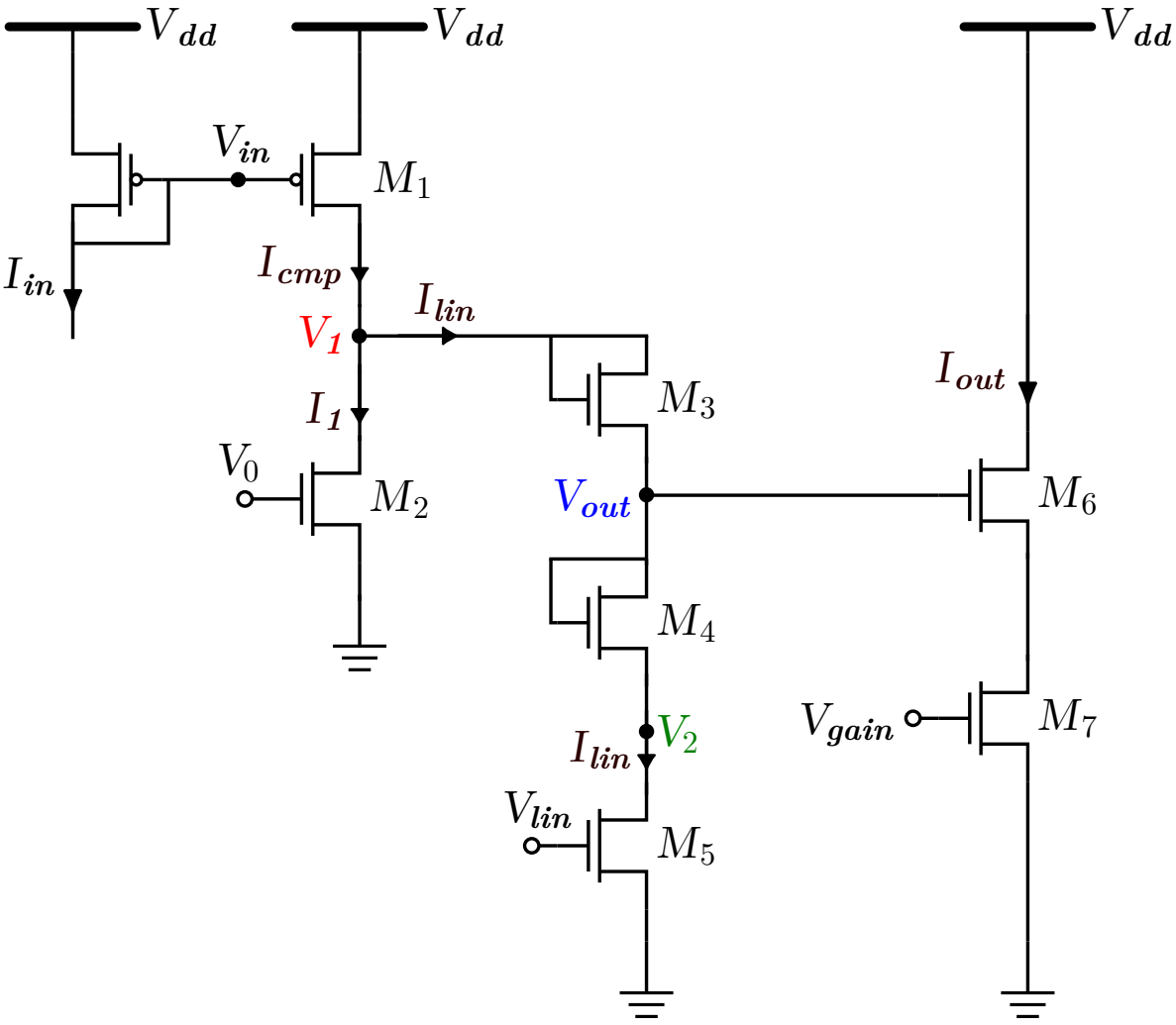


Figure 2.5: Schematic of the Sigmoid circuit designed by Chenxi Wen from the NCS group at the Institute of Neuroinformatics, University of Zurich and ETH Zurich.

2.3.1 Equations

To understand how this circuit works, we'll derive the equations that govern its behavior. Let's start by introducing the general relationship between the gate current and voltage of a transistor used in a diode configuration:

$$V_P, \text{diode}(I) = V_{dd} - \frac{U_T}{\kappa} \log\left(\frac{I}{I_0}\right), \quad V_N, \text{diode}(I) = \frac{U_T}{\kappa} \log\left(\frac{I}{I_0}\right). \tag{2.8}$$

We can now derive the equations governing the circuit's behavior. But first let's modify the sub-threshold equations to facilitate equation manipulation. Equations 2.1 and 2.2 become :

$$\text{Transistor NMOS: } I = I_{n0} e^{\kappa_n V_g - V_s/U_T} \left(1 - e^{-(V_d - V_s)/U_T}\right), \tag{2.9}$$
$$\text{Transistor PMOS: } I = I_{p0} e^{\kappa_p (V_{dd} - V_g) - (V_{dd} - V_s)/U_T} \left(1 - e^{-(V_s - V_d)/U_T}\right). \tag{2.10}$$

Using these equations for each transistor in this circuit, we can express the currents as follows:

$$\text{Transistor M1: } I_{cmp} = I_0 e^{\kappa(V_{dd} - V_{in})/U_T} \left(1 - e^{-(V_{dd} - V_1)/U_T}\right), \tag{2.11}$$
$$\text{Transistor M2: } I_1 = I_0 e^{\kappa V_0/U_T} \left(1 - e^{-V_1/U_T}\right), \tag{2.12}$$
$$\text{Transistor M3: } I_{lin1} = I_0 e^{(\kappa V_1 - V_{out})/U_T} \left(1 - e^{-(V_1 - V_{out})/U_T}\right), \tag{2.13}$$
$$\text{Transistor M4: } I_{lin2} = I_0 e^{(\kappa V_{out} - V_2)/U_T} \left(1 - e^{-(V_{out} - V_2)/U_T}\right), \tag{2.14}$$
$$\text{Transistor M5: } I_{lin3} = I_0 e^{\kappa V_{lin}/U_T} \left(1 - e^{-V_2/U_T}\right). \tag{2.15}$$

Using Kirchhoff's Current Law (KCL) and considering the parasitic capacitance C at each node (V_1, V_{out}, V_2), we establish the following current balance equations:

$$\begin{aligned} \text{Node 1:} \quad & C\frac{dV_1}{dt} = I_{cmp} - I_1 - I_{lin1}, \\ \text{Node 2:} \quad & C\frac{dV_{out}}{dt} = I_{lin1} - I_{lin2}, \\ \text{Node 3:} \quad & C\frac{dV_2}{dt} = I_{lin2} - I_{lin3}. \end{aligned} \tag{2.16}$$

For the sake of clarity, parasite capacity is not shown in the circuit schematic. The I_{lin1}, I_{lin2} and I_{lin3} currents are easily deduced from the circuit schematic, simply by

following the direction of the I_{lin} current in the diagram. In practice, this is a current-driven circuit, and each voltage parameter in the schematic is actually imposed by a current using a current mirror, but representing them would have made the schematic much more cumbersome.

After selecting the four main currents that determine the circuit's operation (I_{in}, I_0, I_{lin} and I_{gain}), we can deduce the corresponding voltages V_{in}, V_0, V_{lin}, and V_{gain} using Equation 2.8. We then solve the following system of differential equations with unknown voltages V_1, V_{out}, and V_2, each associated with specific current values:

$$\begin{aligned}
C\frac{dV_1}{dt} &= I_0 \exp\left(\kappa\frac{V_{dd}-V_{in}}{U_T}\right)\left(1-\exp\left(-\frac{V_{dd}-V_1}{U_T}\right)\right) \\
&\quad - I_0 \exp\left(\kappa\frac{V_0}{U_T}\right)\left(1-\exp\left(-\frac{V_1}{U_T}\right)\right) \\
&\quad - I_0 \exp\left(\frac{\kappa V_1 - V_{out}}{U_T}\right)\left(1-\exp\left(-\frac{V_1-V_{out}}{U_T}\right)\right) \\
C\frac{dV_{out}}{dt} &= I_0 \exp\left(\frac{\kappa V_1 - V_{out}}{U_T}\right)\left(1-\exp\left(-\frac{V_1-V_{out}}{U_T}\right)\right) \\
&\quad - I_0 \exp\left(\frac{\kappa V_{out} - V_2}{U_T}\right)\left(1-\exp\left(-\frac{V_{out}-V_2}{U_T}\right)\right) \\
C\frac{dV_2}{dt} &= I_0 \exp\left(\frac{\kappa V_{out} - V_2}{U_T}\right)\left(1-\exp\left(-\frac{V_{out}-V_2}{U_T}\right)\right) \\
&\quad - I_0 \exp\left(\kappa\frac{V_{lin}}{U_T}\right)\left(1-\exp\left(-\frac{V_2}{U_T}\right)\right)
\end{aligned} \tag{2.17}$$

Solving this system of differential equations gives us the transient response of the circuit, enabling us to determine the relationship between the output and input voltages. The relationship between input current I_{in} and output current I_{out} is then easily found using the following two equations :

$$I_{in}(V_{in}) = I_0 \exp\left(\kappa\frac{V_{dd}-V_{in}}{U_T}\right), \tag{2.18}$$

$$I_{out}(V_{out}) = \frac{I_0 \exp\left(\kappa\frac{V_{out}}{U_T}\right)}{1+\exp\left(\kappa\frac{V_{out}-V_{gain}}{U_T}\right)}, \tag{2.19}$$

where:

- C: Parasitic capacitance at each node (V_1, V_{out}, V_2).

- V_{in}, V_{lin}, V_0 and V_{gain}: Voltages set by the current mirrors through the circuit.

The Equation 2.19 is obtained by writing the Equation 2.9 for transistors M6 and M7, and Equation 2.18 is obtained by rewriting the Equation 2.8 for a PMOS transistor.

2.3.2 Behavior

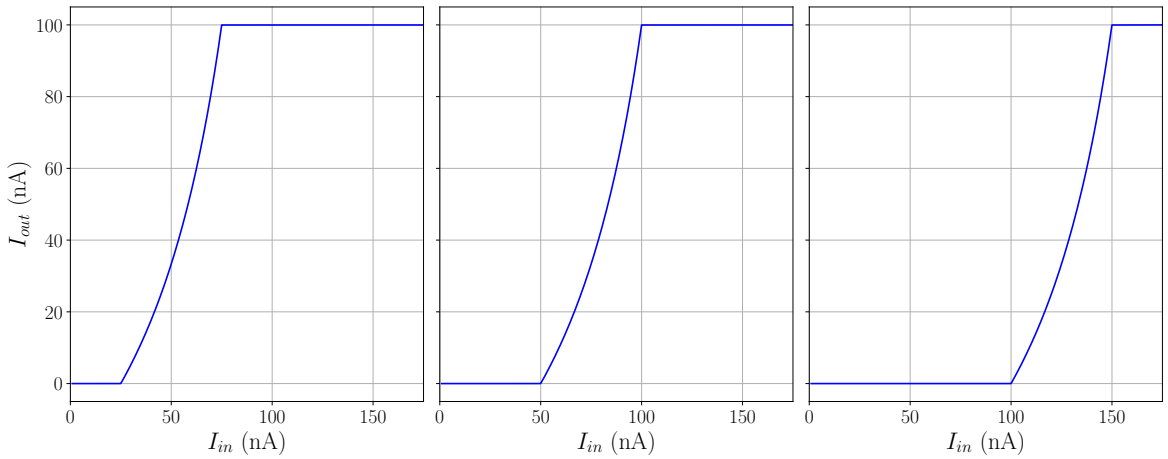
By solving these equations numerically, we can determine the value of I_{out} corresponding to a variation of I_{in}. We used *Julia's BifurcationKit* package to carry out this analysis. As you can see, our simulation result (Figure 2.6) show that the circuit behaves like a sigmoid.

Figure 2.6, shows that if the linear region determined by I_{lin} and I_{gain} is too large, the sigmoid is slightly concave in the linear region. Conversely, if it is too short, the sigmoid is slightly convex in this region.

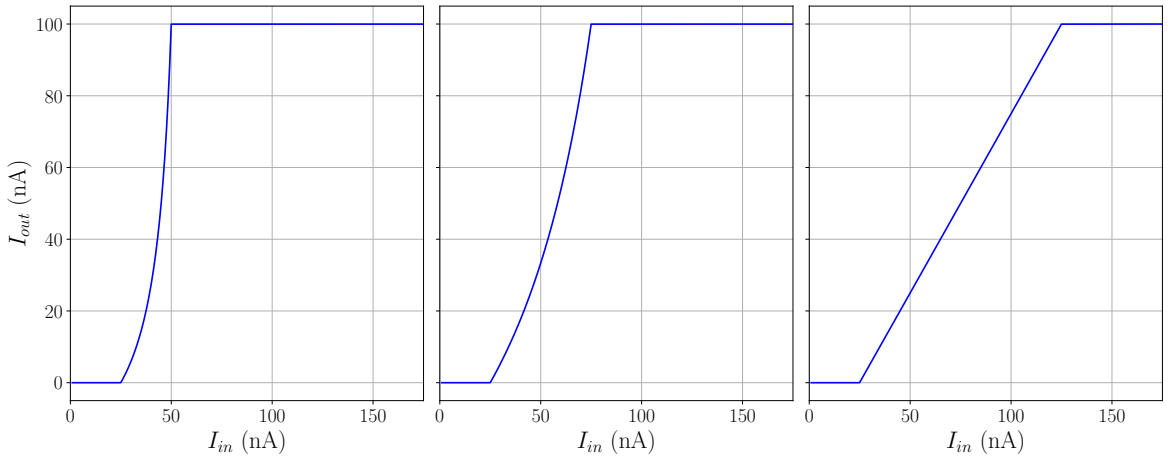
2.3.3 Parameters

In view of the observations we've just made, the key parameters of the sigmoid circuit, interpreted in terms of currents, are:

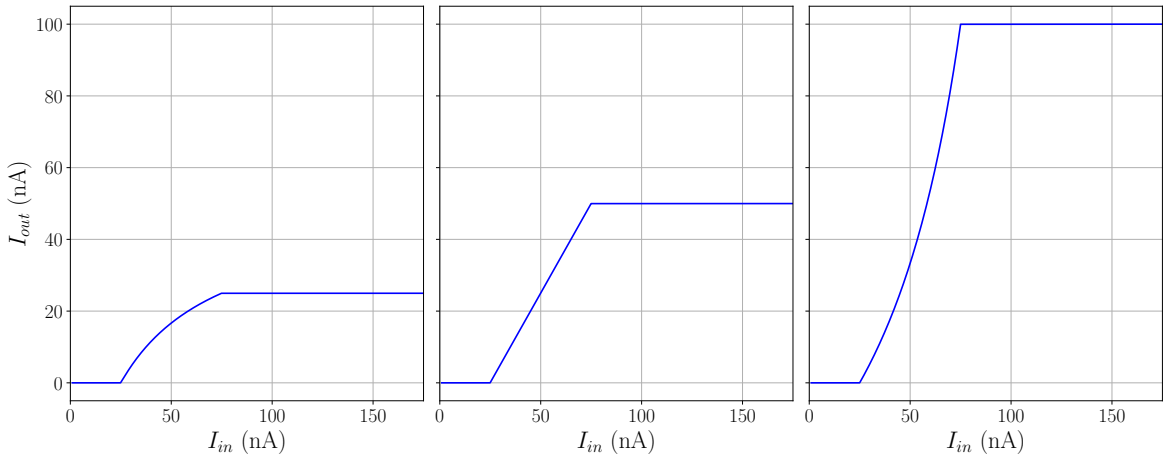
- I_0: Defines the threshold input current I_{in} at which the circuit begins to respond. Increasing I_0 raises the input current needed for I_{out} to start changing, effectively shifting the sigmoid horizontally along the I_{in} axis.
- I_{lin}: Sets the range of input current over which the response is linear, meaning I_{out} is almost proportional to I_{in} within the range $[I_0, I_0 + I_{lin}]$.
- I_{gain}: Determines the maximum output current at saturation. When I_{in} exceeds the linear range, I_{out} approaches its maximum value, which is equal to I_{gain}.



(a) Variation of I_0 (25 nA, 50 nA, 100 nA) with $I_{lin} = 50$ nA, $I_{gain} = 100$ nA



(b) Variation of I_{lin} (25 nA, 50 nA, 100 nA) with $I_0 = 25$ nA, $I_{gain} = 100$ nA



(c) Variation of I_{gain} (25 nA, 50 nA, 100 nA) with $I_{lin} = 50$ nA, $I_0 = 25$ nA

Figure 2.6: Output current of the sigmoid as a function of the input current, showing the effect of varying I_0, I_{lin}, and I_{gain} while keeping the other parameters constant. Simulations are carried out in *Julia* with the *BifurcationKit* tool, using a parasitic capacitance C = 1 mF.

Chapter 3

Theoretical Background on Feedback and Non-linear Systems

In the design of neuromorphic circuits, feedback mechanisms, whether positive or negative, play a fundamental role in modulating system behavior, especially in systems inspired by biological processes. This section introduces key concepts related to feedback, focusing on how a low pass filter interacts with non-linear functions such as the sigmoid to produce complex, biologically inspired behaviors [4].

3.1 Negative Feedback

Negative feedback acts as a stabilizing mechanism that regulates the behavior of a system to minimize deviations from a desired setpoint. It is essential for counteracting small disturbances, such as noise, and restoring equilibrium. Used in neuromorphic circuits, in the context of bursting, negative feedback ensures the return to a stable or silent phase after a burst. This mechanism often operates on a slower time scale than positive feedback, which drives the active burst phase. The interplay between fast positive feedback and slow negative feedback is essential to produce robust and adjustable burst dynamics, but is not the topic here [13]. Negative feedback is essential for tasks requiring precision and regulation..

Mathematically, a typical negative feedback loop can be represented as:

$$y(t) = G(x(t) - H(y(t))), \tag{3.1}$$

where $y(t)$ represents the system's output, $x(t)$ is the input, H is the feedback function,

and G is a function or transformation applied to the combined input and feedback. In simple systems, G may act as a constant gain, but in more complex systems, it can represent a transfer function or a non-linear transformation. This arrangement ensures that deviations in $y(t)$ are minimized, leading to stability.

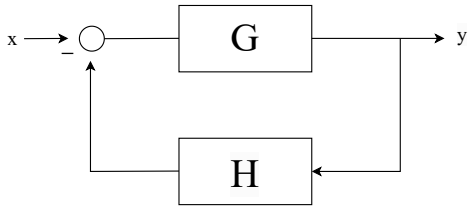


Figure 3.1: Diagram of a negative feedback system.

3.2 Positive Feedback

Positive feedback amplifies deviations from equilibrium, making it essential in systems that require sharp decisions or transitions between states, such as biological neurons. Once a certain threshold is reached, the feedback reinforces the input, pushing the system further from its initial state.

Mathematically, positive feedback can be expressed as:

$$y(t) = G(x(t) + H(y(t))), \tag{3.2}$$

where $y(t)$ represents the system's output, $x(t)$ is the input, H is the feedback function, and G is a function or transformation applied to the combined input and feedback.

One critical feature of systems with positive feedback is hysteresis, where the output depends not only on the current input but also on its past states. This phenomenon is particularly evident when the system transitions between two stable states. As the input $x(t)$ increases, the positive feedback amplifies deviations, causing $y(t)$ to increase rapidly after crossing a specific threshold. Conversely, when $x(t)$ decreases, the system does not immediately return to its initial state. Instead, the output remains in the new state until $x(t)$ falls below a lower threshold. This property is particularly useful in systems requiring stability and memory, as it prevents frequent state transitions in response to small perturbations [4].

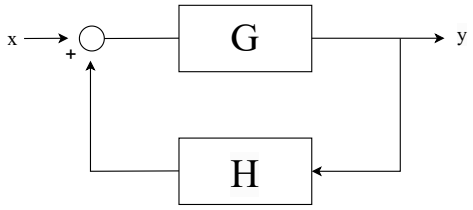


Figure 3.2: Diagram of a positive feedback system.

3.3 Transition from Digital to Analog Representation

To bridge the gap between digital and analog representations in neuromorphic systems, the sigmoid function plays a crucial role. While digital systems operate on discrete values, such as binary signals (0 and 1), analog systems handle continuous variables, enabling more nuanced and gradual responses. In neuromorphic systems, the sigmoid function facilitates the representation of analog dynamics that are fundamental in biological processes, such as gradual state changes and decision-making.

The sigmoid function introduces non-linearity into neuromorphic circuits, enabling smooth transitions between states. This property is essential for systems that need to respond progressively to small changes in input while allowing for sharp transitions once a critical threshold is reached. Such behavior closely emulates biological systems [4].

By facilitating these smooth transitions and enabling gradual responses, the sigmoid function not only enhances the ability of neuromorphic circuits to emulate biological decision-making but also serves as a foundational tool for implementing complex dynamics. These include multistability and gradual state shifts, which are critical for advanced neuromorphic applications [14].

3.4 Low-Pass Filter and Sigmoid for Positive Feedback

Although a low-pass filter is traditionally associated with negative feedback, its combination with the non-linear properties of a sigmoid function can be adjusted to create positive feedback. This configuration allows the system to exhibit bistability [14]. In

this work, we will focus only on positive feedback. Before looking at the dynamics of the final system, let's take a look at the dynamics of the individual blocks.

The Low Pass Filter

The transient response of a low pass filter can be described by the equation:

$$\tau \dot{I}_{out} = -I_{out} + I_{in}, \tag{3.3}$$

with the frequency domain equivalent:

$$H(s) = \frac{1}{\tau s + 1}, \tag{3.4}$$

where:

- τ is the time constant of the system, determining how quickly the system reacts to changes in its input.
- I_{in} is the input of the low pass filter.
- I_{out} is the output of the low pass filter.

The low-pass filter smooths the system's transitions, introducing a temporal delay in its response. While it does not directly cause hysteresis, this delay interacts with positive feedback to shape the system's dynamics, allowing it to transition more gradually between states.

The Sigmoid

The transient response of the sigmoid is defined as:

$$I_{out} = S(I_{in}), \tag{3.5}$$

where:

- $S(x)$ represents the sigmoidal function, typically expressed as:

$$S(x) = \frac{1}{1 + e^{-x}}.$$

  or a similar non-linear function with saturation properties.

- I_{in} is the input to the sigmoid.

- I_{out} is the output of the sigmoid.

The sigmoid introduces sharp transition from low to high output around a critical input value.

Final System Dynamics

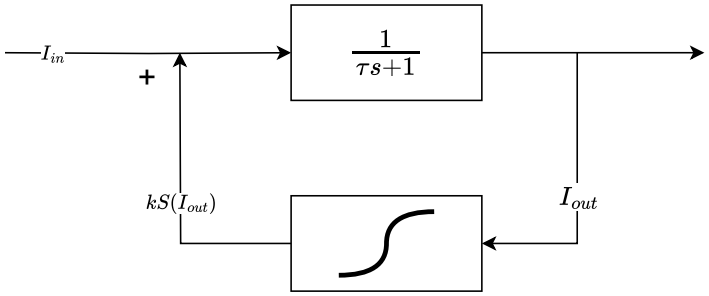


Figure 3.3: Diagram of a sigmoid in positive feedback with a low pass filter.

By combining the low pass filter and the sigmoid in a positive feedback loop, as shown in Figure 3.3, the system dynamics can be described by the following differential equation:

$$\tau \dot{I}_{out}(t) = -I_{out}(t) + k \cdot S(I_{out}(t)) + I_{in}(t) \tag{3.6}$$

This combined system offers rich dynamic behavior. The sigmoid introduces non-linearity, enabling sharp transitions, while the low-pass filter smoothes the system response and introduces temporal delays. Combined with positive feedback, these elements enable the system to exhibit multistability and hysteresis, making it ideally suited to neuromorphic applications.

Role of Each Parameter

- τ**:** Determines the speed of the low-pass filter's response. A larger τ slows down the system's response, making transitions smoother and less abrupt. Conversely, a smaller τ reduces the delay, allowing the system to respond more quickly to changes.
- k**:** Determines the slope and saturation value of the sigmoid function. A higher k leads to sharper transitions and stronger amplification of deviations, while a lower k makes the transitions smoother and less sensitive to noise.
- $I_{in}(t)$ **:** Acts as the external control signal, driving the system's transitions. A slowly varying $I_{in}(t)$ highlights the hysteresis behavior and bistability of the system.
- $S(.)$**:** Provides the non-linearity essential for multistability. Its shape (steepness, threshold, and saturation) directly affects the stability of the states and the transitions between them.
- $I_{out}(t)$**:** Represents the final state of the system, which depends on all the above parameters.

3.5 Pitchfork Bifurcation

Bifurcations are key concepts in the study of nonlinear dynamical systems, describing how the stability and number of equilibrium states change as a control parameter varies. Among these, the *pitchfork bifurcation* is a fundamental type that occurs in systems with symmetry. It is categorized into two main types: *supercritical* and *subcritical* [15]. Additionally, *unfolding* is often used to study perturbations that break the symmetry of the bifurcation.

A pitchfork bifurcation describes how a single equilibrium point splits into multiple equilibria as the control parameter λ crosses a critical value. Depending on the nature of the bifurcation, the stability of the equilibria changes differently as λ crosses this critical value. The value may differ from case to case. For the theoretical part here, we'll consider the normal form with critical value $\lambda = 0$.

3.5.1 Supercritical Pitchfork Bifurcation

In a *supercritical pitchfork bifurcation*, a single stable equilibrium becomes unstable, and two new stable equilibria symmetrically emerge as the bifurcation parameter λ increases beyond a critical value. This type of bifurcation is smooth and continuous. It can be described by the following equation :

$$\frac{dx}{dt} = \lambda x - x^3. \tag{3.7}$$

Where x is the state variable and λ is the bifurcation parameter.

- For $\lambda < 0$, the system has one stable equilibrium at $x = 0$.
- For $\lambda > 0$, the equilibrium at $x = 0$ becomes unstable, and two stable equilibria appear at $x = \pm\sqrt{\lambda}$.

The bifurcation diagram for a supercritical pitchfork bifurcation is shown in Figure 3.4.

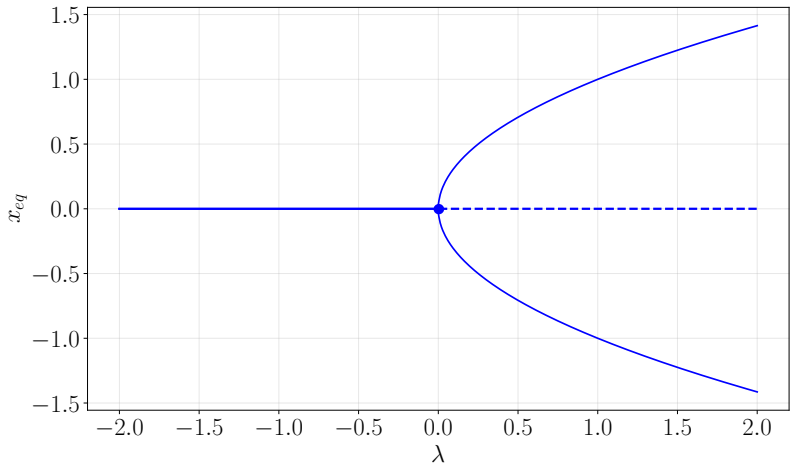


Figure 3.4: Bifurcation diagram for a supercritical pitchfork bifurcation. The solid lines indicate stable equilibria, and the dashed line indicates an unstable equilibrium.

3.5.2 Subcritical Pitchfork Bifurcation

In a *subcritical pitchfork bifurcation*, we have a single stable equilibrium and two symmetric unstable equilibria for $\lambda < 0$. As λ increases beyond the critical point ($\lambda > 0$), the unstable equilibria disappear, leaving only an unstable equilibrium at $x = 0$. This type of bifurcation is described by the following equation:

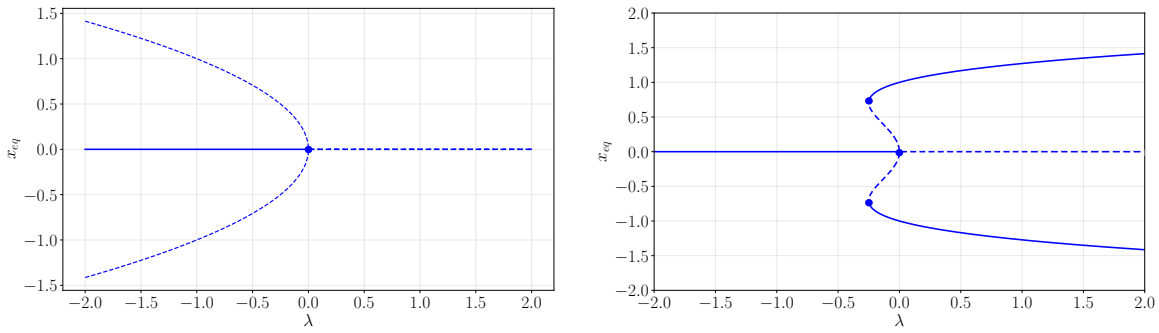
$$\frac{dx}{dt} = \lambda x + x^3. \tag{3.8}$$

- For $\lambda < 0$, the equilibrium at $x = 0$ is stable and there is two unstable equilibra at $x = \pm\sqrt{-\lambda}$.
- For $\lambda > 0$ the equilibrum at $x = 0$ is unstable.

In practice we can have a stabilizing term which will prevent divergent solutions for high values of $|x|$ which gives [16] :

$$\frac{dx}{dt} = \lambda x + x^3 - x^5, \tag{3.9}$$

where x^5 is the stabilizing term. In the range $\lambda_s < \lambda < 0$, where λ_s corresponds to the point at which the two stable branches emerge, multiple qualitatively different stable states coexist. The initial condition x_0 determines which fixed point is approached as $t \to \infty$. The existence of different stable states allows for the possibility of jumps and hysteresis as λ is varied. The bifurcation at $\lambda_s = -0.25$ marks a saddle-node bifurcation. The bifurcation diagram for a subcritical pitchfork bifurcation is shown in Figure 3.5. [17]



(a) Bifurcation diagram for a subcritical pitchfork bifurcation without stabilizing term.

(b) Bifurcation diagram for a subcritical pitchfork bifurcation with stabilizing term.

Figure 3.5: Bifurcation diagram for a subcritical pitchfork bifurcation with and without stabilizing term. The solid lines indicate stable equilibria, and the dashed lines indicate unstable equilibria.

3.5.3 Unfolding of the Pitchfork Bifurcation

The *unfolding* of a pitchfork bifurcation refers to the analysis of perturbations that break the symmetry of the bifurcation.

A common way to model unfolding is to add an asymmetry term (ϵ). For example, in the case of the supercritical pitchfork with Equation 3.9 it gives :

$$\frac{dx}{dt} = \lambda x + x^3 - x^5 + \epsilon, \tag{3.10}$$

for $\epsilon \neq 0$, the symmetry of the bifurcation is broken, and one of the stable equilibria becomes dominant.The bifurcation diagram for an unfolded subcritical pitchfork bifurcation is shown in Figure 3.6.

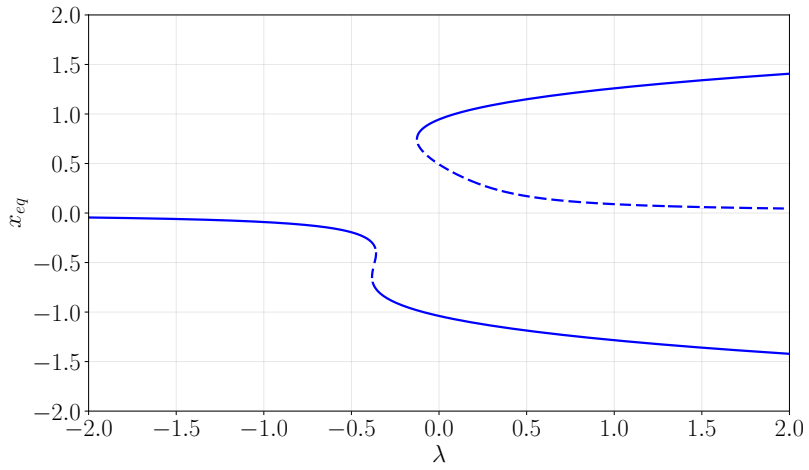


Figure 3.6: Bifurcation diagram for an unfolded pitchfork bifurcation, illustrating the impact of the asymmetry parameter $\epsilon = 0.09$. The solid lines indicate stable equilibria, and the dashed lines indicate unstable equilibria.

Chapter 4

Fast and Flexible decision making

4.1 Introduction

In the nonlinear dynamic systems presented above, sigmoidal functions and their associated bifurcations play a central role in the understanding and design of systems exhibiting complex behaviors such as multistability and hysteresis. As explained, sigmoidal functions, characterized by smooth saturation and nonlinearity, are widely used to model the behavior of systems that exhibit abrupt transitions between states. We've just seen that one of the main types of nonlinear behavior that can appears in such systems is pitchfork bifurcation, which is fundamental to describing how a system moves from one stable state to another when a control parameter is changed [6].

In the context of neuromorphic engineering, where circuits are designed to emulate the behavior of biological neurons and neural systems, reproducing these nonlinear dynamics in hardware is essential but not always straightforward. In the system we're studying, sigmoidal functions and the associated study of bifurcations are particularly relevant for mimicking and understanding the decisional and multistable behaviors observed in biological systems. However, implementing these dynamics in CMOS circuits presents challenges due to practical constraints. In particular, the implementation of the sigmoidal function in CMOS implementations means that we have a sigmoid that is not symmetrical around zero as in other work [6], since it generally only operates in the positive quadrant due to the unipolar nature of standard CMOS circuit designs.

In this chapter, we explore the impact of these challenges on the design and dynamics of neuromorphic circuits. Specifically, we analyze how the absence of a symmetric sigmoidal function around zero affects multistability conditions. Despite the constraints of unipolar sigmoidal functions, we demonstrate that it is still possible to replicate the key behaviors observed in systems with a symmetric sigmoid (around zero) by leveraging CMOS circuit designs. Additionally, we examine the impact of using a double sigmoid instead of a single sigmoid on the system's dynamics. In the following section, we analyze the bifurcation equations and describe the changes introduced by using single and double sigmoids. The results of these analyses are then discussed.

4.2 Bifurcation Analysis

As explained in the previous chapter, bifurcation analysis plays a crucial role in understanding the dynamic behaviour of non-linear systems. In these systems, bifurcations describe how small variations in parameters can lead to qualitative changes in the equilibrium states of the system.[6]

This section begins with a theoretical analysis of bifurcation, focusing on the general conditions necessary for bifurcation to occur in our nonlinear systems that use a uniquely defined sigmoid function in the positive quadrant in positive feedback with a low-pass filter. Next, we apply the theoretical framework to two specific cases: first, we study the supercritical pitchfork bifurcation induced by a single sigmoid function, and then we explore the subcritical pitchfork bifurcation induced by a double sigmoid function. In both cases, we examine the role of key parameters such as the slope and horizontal displacements of the sigmoid functions in the formation of the bifurcation.

Starting from Equation 3.6, we can rewrite the equation governing the behavior of our system in the following form:

$$\dot{I}_{out} = \frac{1}{\tau}(-I_{out} + k \cdot S(I_{out}) + I_{in}(k)), \tag{4.1}$$

where $I_{in}(k) = I_{in,1} + k \times I_k$ represents the system's input current. The equation remains the same as before, except that the input current now depends on k , allowing the equilibrium point to remain fixed as k varies. This term is introduced solely for theoretical analysis. Thus, the input current can be decomposed into two components:

- $I_{in,1}$ is the actual input current of the system.
- I_k represents a shift in the sigmoid, adjusting the equilibrium position.

The mathematical development is based on the following key equation governing the dynamics:

$$F(I^*_{out}(k), k, I_{in}(k)) = 0, \tag{4.2}$$

where F is the function describing the system equilibrium, $I^*_{out}(k)$ is the equilibrium state as a function of the bifurcation parameter k. Given this equation, to analyze the system's bifurcation behavior, we simply need to consider the equilibrium condition first:

$$F(I_{out}(k), k, I_{in}(k) = \frac{1}{\tau}\left(-I_{out} + k \cdot S(I_{out}) + I_{in}(k)\right) = 0. \tag{4.3}$$

By differentiating $F(I^*_{out}(k), k, I_{in}(k))$ with respect to k, we derive the equation governing the evolution of the equilibrium $I^*_{out}(k)$ as k varies. The total derivative of F with respect to k is:

$$\frac{dF}{dk} = \frac{\partial F}{\partial k} + \frac{\partial F}{\partial I_{out}} \cdot \frac{dI^*_{out}}{dk} + \frac{\partial F}{\partial I_{in}} \cdot \frac{dI_{in}(k)}{dk} = 0, \tag{4.4}$$

where:

$$\frac{\partial F}{\partial k} = S(I_{out}), \quad \frac{\partial F}{\partial I_{out}} = -1 + k \cdot S'(I_{out}), \quad \frac{\partial F}{\partial I_{in}} = 1, \quad \frac{dI_{in}(k)}{dk} = I_k. \tag{4.5}$$

Solving for $\frac{dI^*_{out}}{dk}$, we obtain the following equation:

$$\begin{aligned} \frac{dI^*_{out}}{dk} &= -\left(\frac{\partial F}{\partial I_{out}}\right)^{-1}\left[\frac{\partial F}{\partial k} + \frac{\partial F}{\partial I_{in}}\frac{dI_{in}(k)}{dk}\right] \\ &= -\left(\frac{1}{k \cdot S'(I_{out}) - 1}\right)\left[S(I_{out}) + I_k\right]. \end{aligned} \tag{4.6}$$

This expression shows how the equilibrium $I^*_{out}(k)$ evolves as the bifurcation parameter k changes, taking into account the nonlinear sigmoid term $S(I_{out})$ and the input term I_k.

4.2.1 Simple Sigmoid

Now that we've seen how equilibrium evolves as a function of sigmoid gain, let's examine the case of a simple sigmoid similar to the one in our circuit. The mathematical expression for the sigmoid is given by:

$$S(x) = \frac{1}{1 + e^{-k_0(x-x_0)}}.$$

Here, k_0 determines the steepness of the sigmoid, and x_0 represents the inflection point (or horizontal shift). To ensure the sigmoid aligns with the dynamics of the low-pass filter (LPF), which is characterized by the linear slope $I_{out} = I_{in}$, the parameters k_0 and x_0 must be carefully selected.

Alignment Condition

To ensure alignment, the slope of the sigmoid at its symetry point (in this case the inflection point) must match the LPF's linear response. Mathematically, this condition is satisfied when the derivative of the sigmoid, $S'(x)$, at x_0, equals 1. The derivative is given by:

$$S'(x) = \frac{k_0 e^{-k_0(x-x_0)}}{(1 + e^{-k_0(x-x_0)})^2}.$$

By setting $x_0 = 1.5$ and solving the above equation for $S'(x_0) = 1$, we find:

$$k_0 = 4.$$

Determining $I_{in,1}$ and I_k

To fully align the sigmoid with the LPF dynamics, we next determine the values of $I_{in,1}$ and I_k. The alignment must satisfy two conditions:

1. The symmetry point x_0 must satisfy the following conditions to be aligned with the LPF dynamics :
$$S(x_0) + I_k + I_{in,1} = x_0.$$

2. An additional constraint derived from the system dynamics must hold see Equation 4.6:

$$\frac{1}{k \cdot S'(x_0) - 1} \cdot [S(x_0) + I_k] = 0.$$

Solving these equations gives:

$$I_k = -0.5, \quad I_{in,1} = 1.5.$$

Remark

This process ensures the sigmoid is perfectly aligned with the LPF and defines the conditions under which a pitchfork bifurcation occurs. At the bifurcation point, the system transitions from a single stable equilibrium to two symmetric equilibria, as the sigmoid slope aligns with the LPF's linear behavior at x_0.

While precise, this approach is unnecessarily complex if the exact bifurcation point is not critical. Once x_0, I_k, and $I_{in,1}$ are determined, the bifurcation diagram can reveal the value of k where the bifurcation occurs, provided k is varied over a sufficiently wide range. Here, the definition of k_0 just allows us to ensure that the value of k at the bifurcation point is 1.

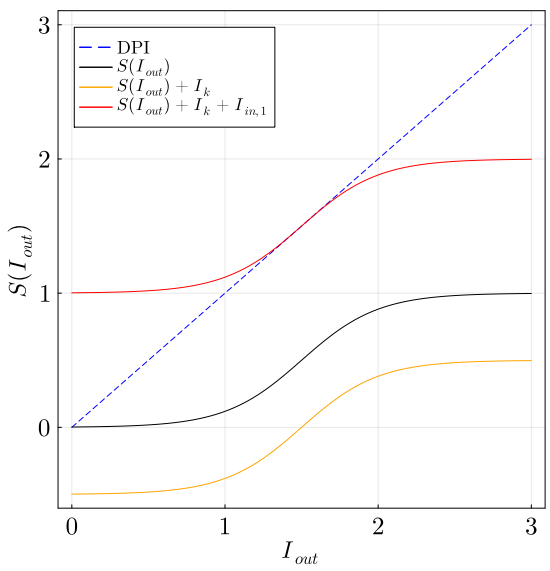
In this context, k_0 becomes less critical, because it only defines the initial slope of the sigmoid. The parameter k, on the other hand, plays a central role, affecting both the gain and the slope of the sigmoid. Thus, we only need to ensure that the sigmoid is symmetrically aligned with the LPF to capture the system's bifurcation dynamics. In other words, the point of symmetry of the sigmoid must lie on the line $I_{out} = I_{in}$.

Results

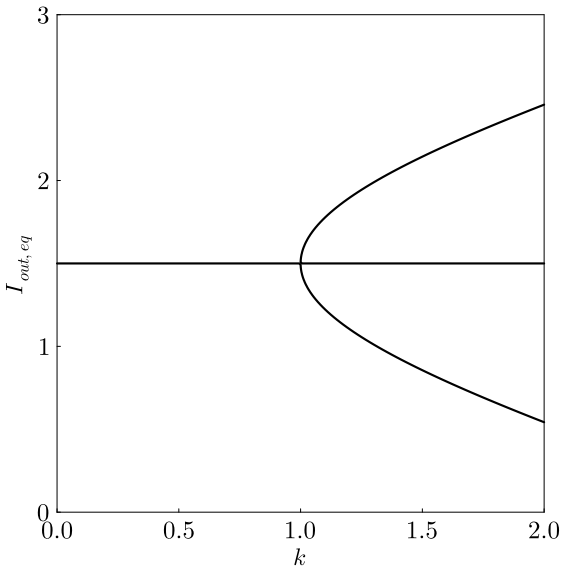
The bifurcation diagram in Figure 4.1b illustrates the transition of the system from one stable state to two symmetric states as soon as k exceeds the critical value of 1, confirming the presence of a pitchfork bifurcation.

Figures 4.1c and 4.1d illustrate a phenomenon of hysteresis observed in the system. In these two figures, to show the hysteresis, we've chosen k = 2 to get into the bistable region. The hysteresis observed is due to the interaction between the positive feedback and the non-linearity of the sigmoid. The sigmoid introduces thresholds for the transitions, while the positive feedback amplifies small deviations, allowing the system to maintain its state even when the input crosses back over the threshold.

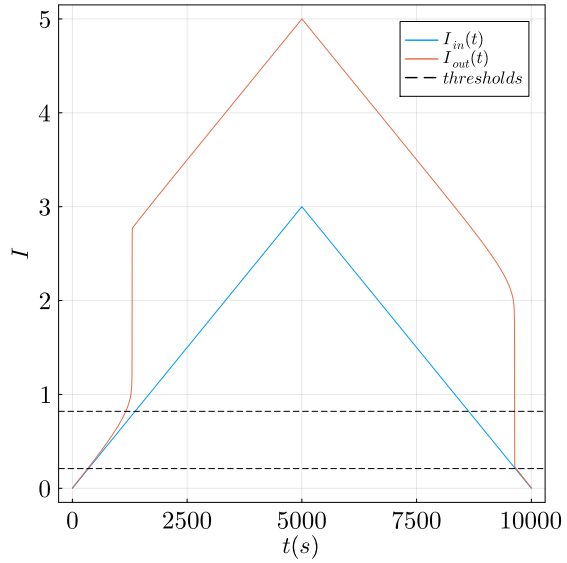
The low-pass filter, while not responsible for the hysteresis itself, modulates the dynamics of the transitions by introducing temporal inertia. For larger time constants (τ), transitions are smoother, while for smaller τ , transitions become more abrupt. This temporal smoothing can make the hysteresis more apparent during slow input current variations in both directions, as it prevents immediate transitions and allows memory-dependent dynamics to dominate, especially when the time constant is relatively high. In our simulations, the time constant is set to 1, so the input current varies over a long period of time (see Figure 4.1c).



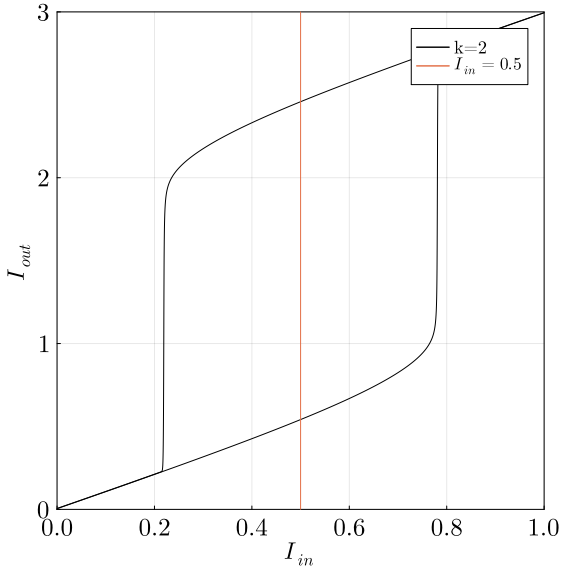
(a) Simple sigmoid function transitions.



(b) Pitchfork bifurcation diagram.



(c) System response to a triangular input.



(d) Hysteresis loop.

Figure 4.1: Analysis of the simple sigmoid function and its associated supercritical pitchfork in the context of positif feedback with a low pass filter.

4.2.2 Double Sigmoid

In the case of the double sigmoid function, the system exhibits more complex nonlinearity, which can lead to a subcritical pitchfork bifurcation. The double sigmoid function is defined as:

$$S(x) = \frac{1}{1 + e^{-k_1(x-x_1)}} + \frac{1}{1 + e^{-k_2(x-x_2)}}.$$

Where k_1 and k_2 control the steepness of each sigmoidal transition, and x_1 and x_2 represent the horizontal shifts of each term. This function combines two sigmoidal responses, resulting in a more complex curve, especially near critical points.

Alignment Condition

We saw in the case of a simple sigmoid the procedure to follow. Here we're going to proceed a little differently, to avoid lengthy mathematical developments, and since the value at which the bifurcation point is located is not important, what we want to do is simply observe the behavior. We'll start from the same base as in the case of the simple sigmoid and align our double sigmoid so that its symmetry point belongs to the $I_{out} = I_{in}$ line that defines the LPF dynamics.

Determining $I_{in,1}$ and I_k

For example, what we can do is set the values of $x_1 = 1.5$ and $x_2 = 2.5$. In this case, the point of symmetry will be located at x = 2. Next, we'll choose k_1 and k_2, which are good starting candidates. Remember, this isn't really the most important choice, since we're varying k. Here, we'll choose $k_1 = k_2 = 8$ because we have well-marked transitions and we're close to $I_{out} = I_{in}$. So now we need to find the values of $I_{in,1}$ and I_k. As before, the point of symmetry must satisfy two constraints:

1. The symmetry point must satisfy the following conditions to be aligned with the LPF dynamics :
$$S(x = 2) + I_k + I_{in,1} = 2.$$
2. An additional constraint derived from the system dynamics must hold:
$$\frac{1}{k \cdot S'(2) - 1} \cdot [S(2) + I_k] = 0.$$

Solving these equations gives:

$$I_k = -1, \quad I_{in,1} = 2.$$

The reason why the symmetry point is always the focal point of our analysis is because it's the only point that won't move when k is varied.

Results

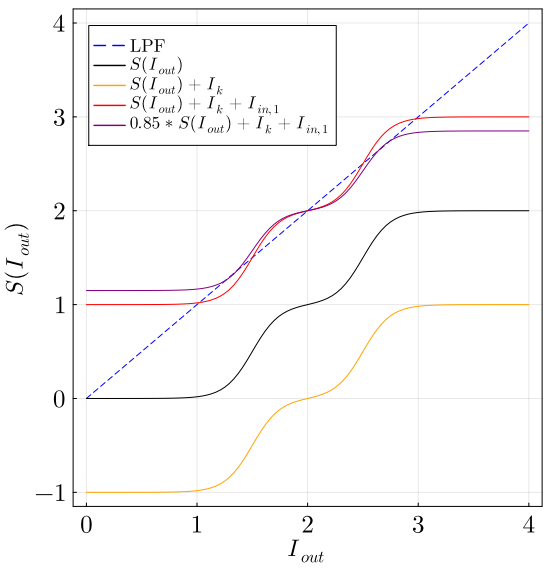
The subcritical pitchfork bifurcation, as shown in Figure 4.2b, exhibits a more abrupt transition compared to the standard pitchfork bifurcation. In such a system, metastable states may arise before the system ultimately settles into one of the two stable branches. This behavior is characteristic of systems with strong nonlinearities. For carefully chosen parameter values, such as $k = 0.85$ in this case, the system can enter a multistable regime with three equilibrium states for certain values of I_{in} (as illustrated in Figure 4.2d and Figure 4.2b). This means that, with sufficiently large perturbations, the system can transition between one equilibrium state and two other distinct equilibrium states. We can see that this configuration corresponds to a double sigmoid which is tangent at two points to the low-pass filter dynamics and intersects the dynamics at a single point, that of the symmetry point (see Figure 4.2a).

Furthermore, altering the parameters of the double sigmoid function, such as increasing the "flat" region after the first sigmoid (thus breaking the symmetry) by adjusting x_2 (e.g., setting $x_2 = 3.5$ instead of $x_2 = 2.5$, as shown in Figure 4.3a), significantly changes the system's behavior. For the same value of k, this modification leads to a fundamentally different regime. In terms of the bifurcation diagram, this adjustment results in an unfolding of the subcritical pitchfork bifurcation, as shown in Figure 4.3b. This unfolding reduces the tristable[1] region to a bistable region, where only two stable equilibria exist.

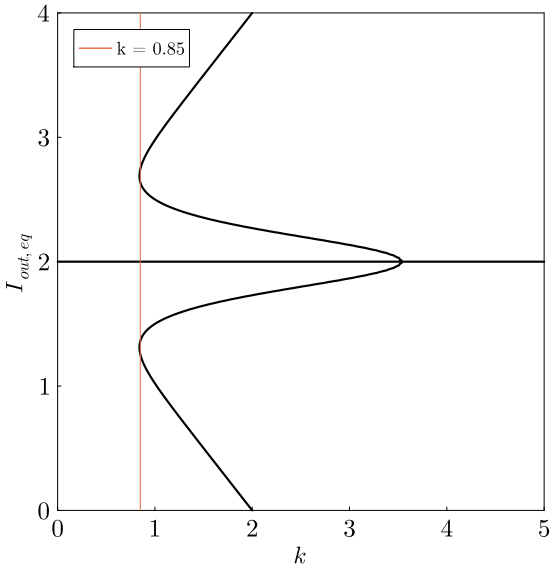
Additionally, examining the hysteresis curve reveals that, while the system exhibits bistability similar to the single sigmoid case, the presence of the double sigmoid introduces two distinct bistable regions depending on the chosen value of I_{in} . Indeed, as shown in the system's response to a triangular input (Figures 4.3c and 4.3d). However, this behavior is solely the result of I_{in} transitioning progressively between two separate bistable regions created by each of the 2 sigmoid. .

[1]The term tristability/tristable will be used in the remainder of this work to designate a multistable region with three different equilibria.

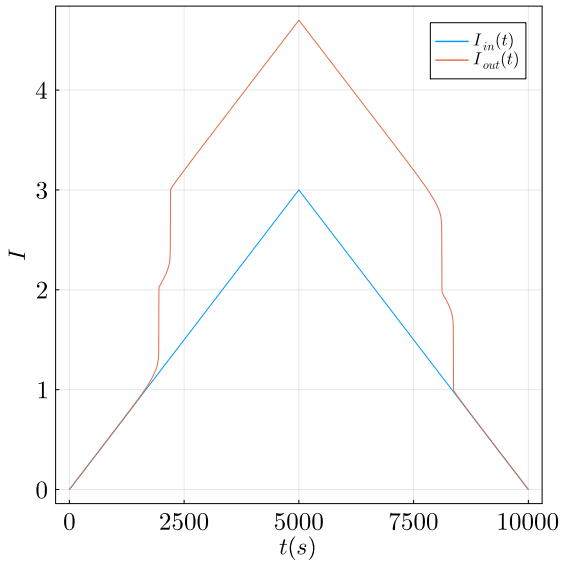
The bifurcation diagrams (figures 4.2b and 4.3b) illustrate how the introduction of the double sigmoid function adds complexity to the dynamics, making the system highly sensitive to parameter changes and leading to more complex bifurcation behavior.



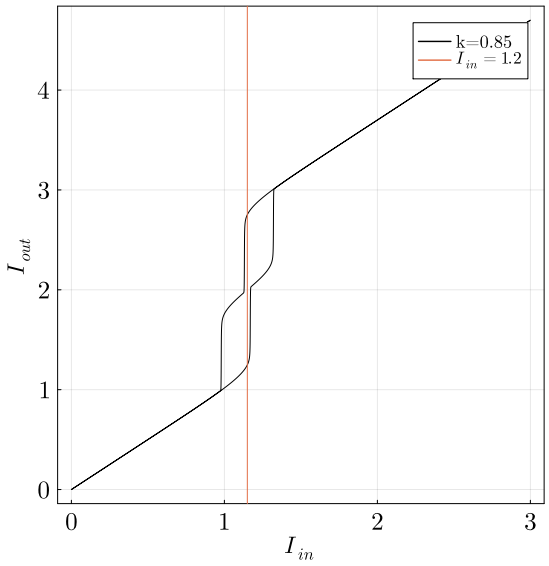
(a) Double sigmoid function transitions.



(b) Subcritical pitchfork bifurcation diagram.

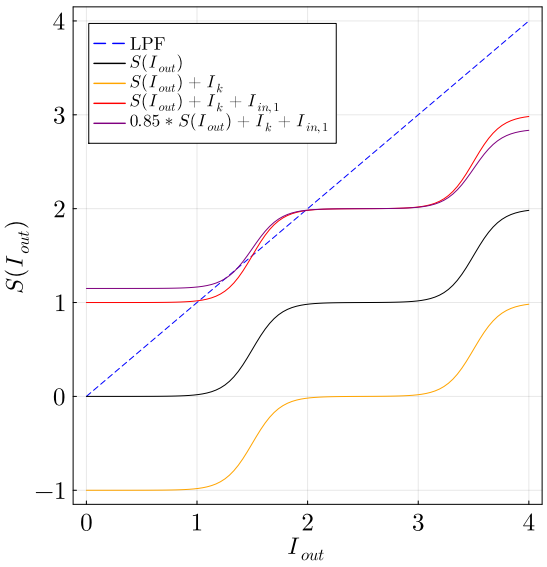


(c) System response to a triangular input.

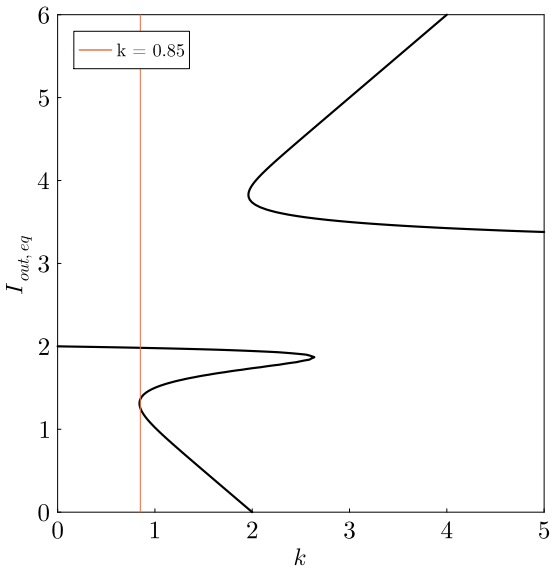


(d) Hysteresis loop.

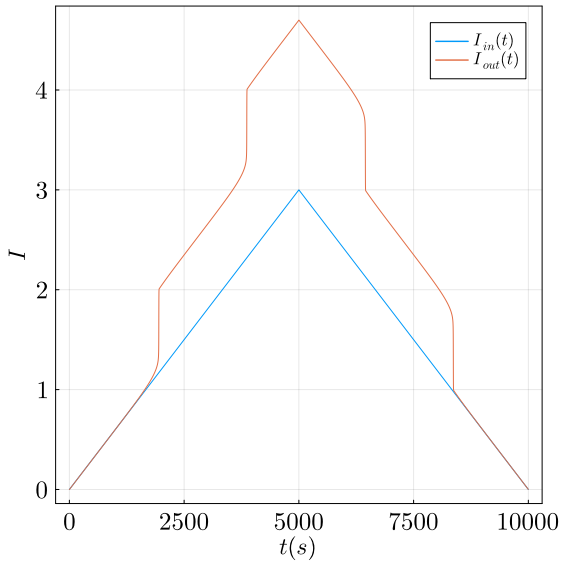
Figure 4.2: Analysis of the double sigmoid function and its associated subcritical pitchfork bifurcation in the context of a positif feedback with a low pass filter.



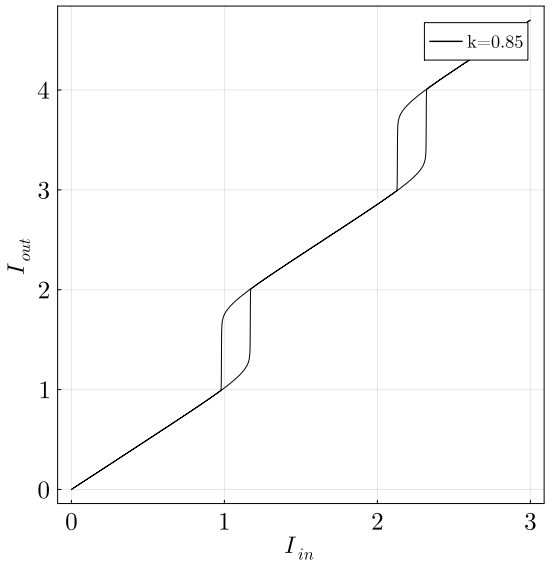
(a) Double sigmoid function transition.



(b) Unfolded subcritical pitchfork bifurcation diagram



(c) System response to a triangular input.



(d) Double hysteresis loop.

Figure 4.3: Analysis of the double sigmoid function and its associated **unfolded** subcritical pitchfork bifurcation int the context of a positive feedback with a low pass filter.

Chapter 5

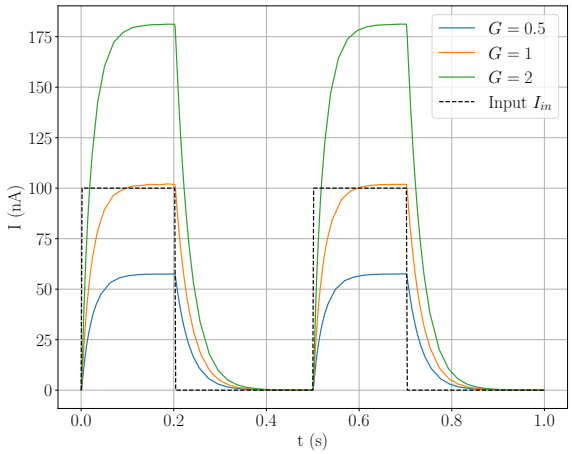
Bistable Modeling for CMOS Applications

In this chapter, we present the *Cadence* implementation of the two circuits presented in Chapter 1, i.e. the sigmoid and DPI circuits. At the end, we'll do the *Cadence* implementation of the sigmoid in positive feedback with the DPI, which will give us a bistable cell. We'll analyze the differences between theoretical and actual behavior.

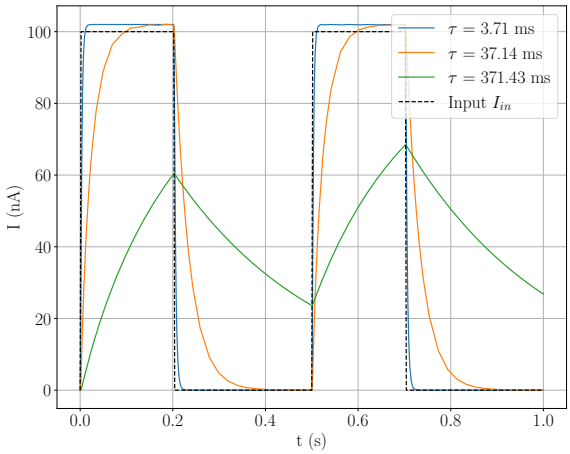
5.1 DPI Circuit Implementation in *Cadence*

The differential pair integrator (DPI) has been implemented in *Cadence* based on the circuit presented in Chapter 2. Configured with appropriate values for G, I_τ, and C, the circuit achieves a stable response with a tunable time constant τ, demonstrating its functionality as an integrator and low-pass filter. We performed *Cadence* simulations using the same parameters and configurations as in the theoretical analysis to validate the correct operation of the circuit.

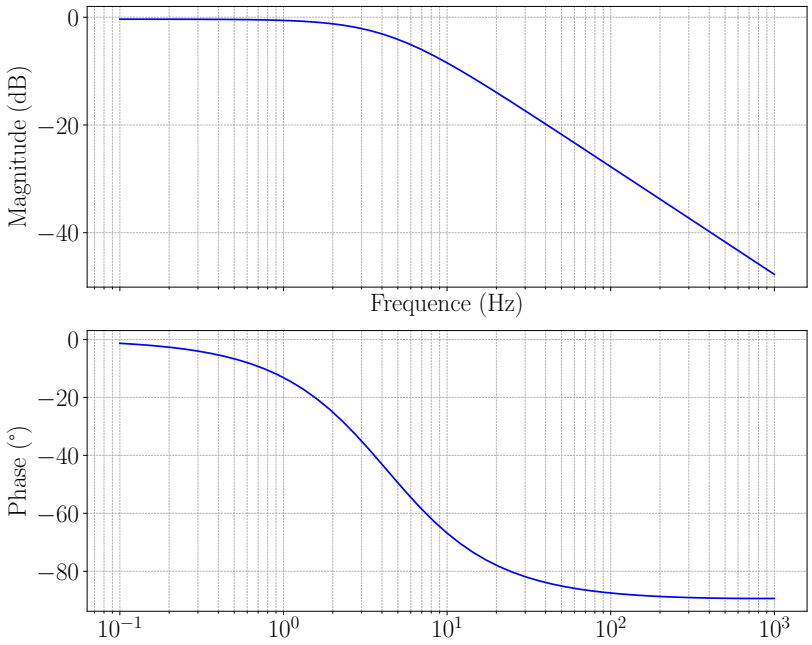
The simulation results are shown in Figure 5.1. The DPI exhibits the expected low-pass filtering behavior, smoothing variations in the input current I_{in} by integrating it over time. The output current I_{out} varies more or less rapidly as a function of the time constant, in good agreement with theoretical predictions. Minor discrepancies in gain values are attributed to transistor non-idealities. These discrepancies are mostly present for gains other than 1. These deviations have minimal impact, since a gain of $G = 1$ is used in subsequent applications.



(a) DPI input/output response for $G = 1$, $G = 2$, and $G = 0.5$ with $C = 70\,\text{pF}$.



(b) DPI input/output response for $C = 7\,\text{pF}$, $C = 70\,\text{pF}$, and $C = 700\,\text{pF}$ with $G = 1$.



(c) Bode diagram of the DPI for $G = 1$ and $C = 70\,\text{pF}$, illustrating the frequency response.

Figure 5.1: Simulated behavior of the DPI using *Cadence*, with all simulations assuming $I_\tau = 70\,\text{pF}$. The transient response is simulated with a rectangular input signal of 100 nA amplitude and a 40% duty cycle.

The Bode plot (Figure 5.1c) confirms the expected frequency response, with a cutoff frequency determined by τ. The Bode diagram shows a cutoff frequency approximately

equal to that predicted in the theoretical analysis:

$$f_c = \frac{1}{2\pi\tau} \approx 4\,\text{Hz}.$$

5.2 Sigmoid Circuit Implementation in *Cadence*

The sigmoid block was implemented in *Cadence*. The parameters I_0, I_{lin}, and I_{gain} were calibrated to match the expected sigmoid behavior:

Figure 5.3 compares the output of the sigmoid block obtained from Cadence simulations with the numerical results of *Julia's BifurcationKit*. The results show that the circuit closely follows theoretical predictions, with minor deviations. These deviations can be attributed to parasitic capacitances and transistor non-idealities. The differences we notice are that the linear region is slightly wider than theoretically expected, saturation is reached more gradually and the observed gain is systematically higher than predicted. Also noteworthy is the fact that parasitic capacitances in the simulations are higher than in reality, to ensure convergence of the numerical simulation.

The shape of the supposedly linear region depends on the choice of I_{gain} and I_{lin} , which can make the region more or less curved. By carefully adjusting these parameters, the impact of some non-idealities can be minimized, as illustrated in Figure 5.2. In general, it is advisable to avoid extending the linear region to very high values, especially when the gain is low. However, these deviations remain minimal within the region of interest for observing multistability.

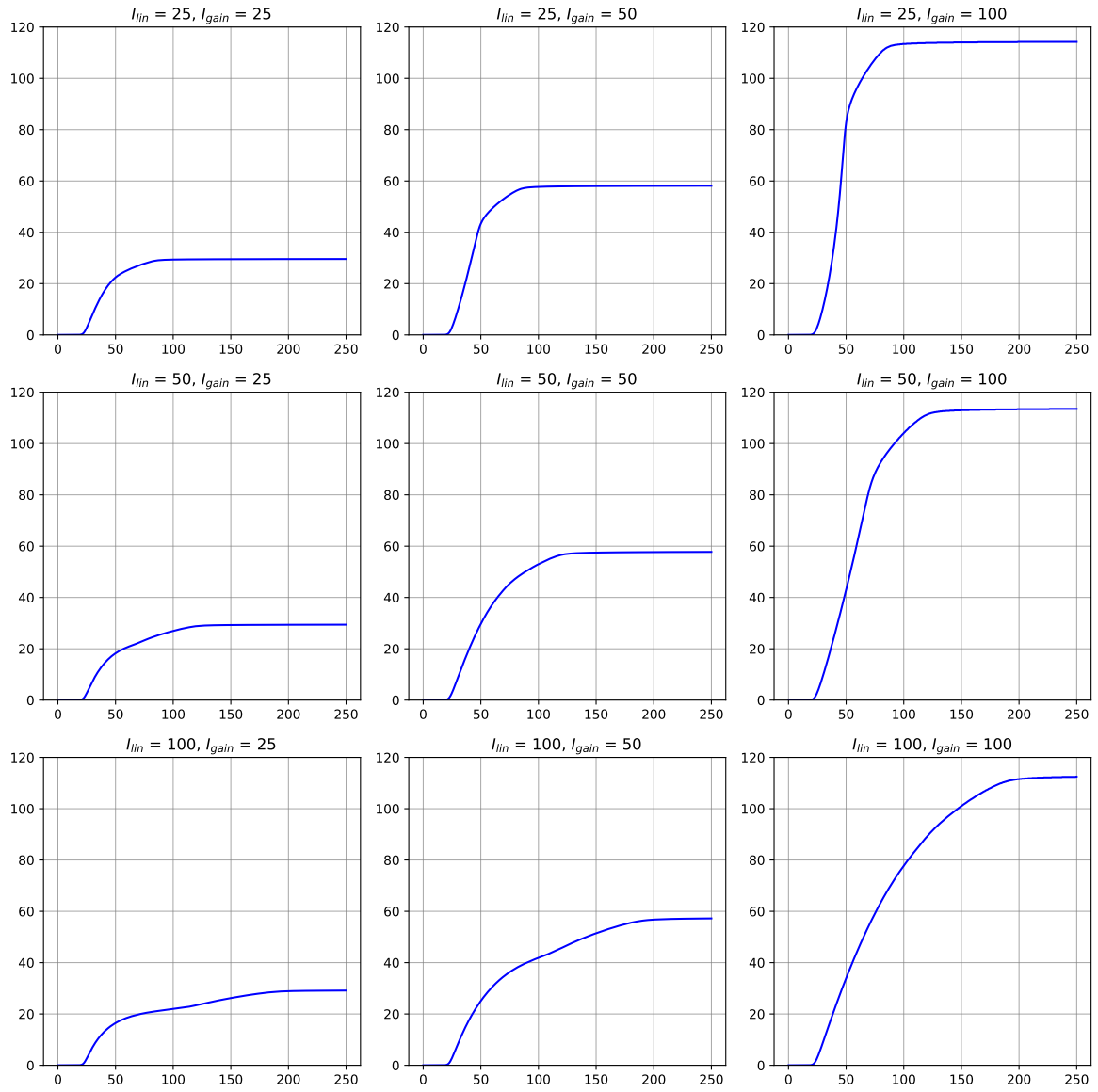


Figure 5.2: Representation of sigmoid curves for different combinations of parameters I_{lin} and I_{gain}. The columns vary with I_{lin}, and the rows vary with I_{gain}. The parameter I_0 is fixed at 25 nA for all plots. The Y-axis represents the output current of the sigmoid in nA, while the X-axis represents the input current to the sigmoid, also in nA. For clarity, axis labels and ticks are omitted. The Y-axis is limited to a maximum value of 120 nA to enhance readability.

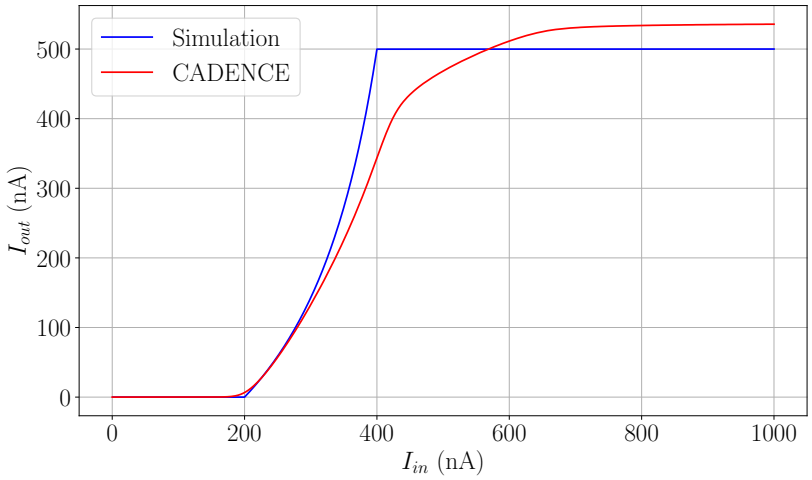


Figure 5.3: Comparison of sigmoid output current versus input current. The graph highlights the differences between a numerical result using *BifurcationKit* and a Cadence simulation, with $I_{gain} = 500$ nA, $I_{lin} = 200$ nA, and $I_0 = 200$ nA.

5.3 Bistable Circuit Analysis

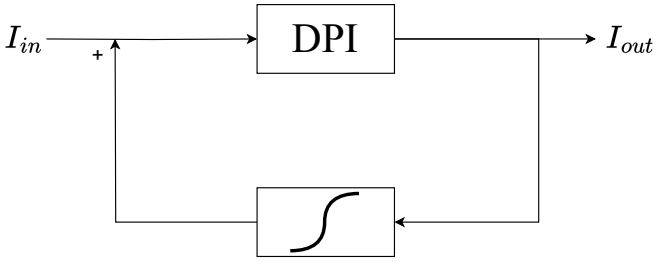


Figure 5.4: Diagram of the bistable circuit combining DPI and sigmoid blocks in a positive feedback configuration.

This section studies the bistable behavior of a circuit combining an DPI and a sigmoid block. The system operates by positive feedback, with the output of the DPI routed to the input of the sigmoid block, forming a feedback loop. This configuration, implemented in *Cadence*, enables the system to stabilize in one of two equilibrium states as a function of input current I_{in} and initial conditions.

5.3.1 Objectives and Experimental Approach

The goal of this section is to explore the bistable dynamics of the DPI-sigmoid circuit and validate its nonlinear behaviors through simulation. As *Cadence* does not natively generate bifurcation diagrams, other methods have been employed to demonstrate this bistable behavior. The various tests performed are as follows:

- **Input current variations** to analyze transitions and bistability behavior in relation to input current.
- **Initial condition variations** to study the sensitivity of equilibrium states.
- **Hysteresis properties** to confirm the robustness of bistability.

5.3.2 Results and Discussion

In this section, we will present and discuss the results of the various tests carried out to characterize the circuit's behavior.

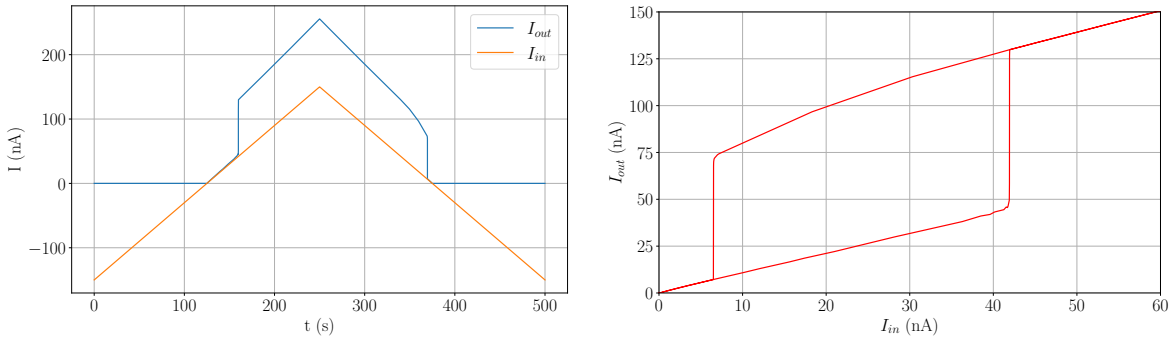
Behavioral Insights

The bistable circuit exhibits transitions between two stable equilibrium states as I_{in} crosses thresholds. Figure 5.5a shows the time evolution of I_{in} and I_{out}, highlighting the system's hysteretic response.

Effect of input current variations

In this section, we use a 300 ms pulse of varying amplitude as input to trigger transitions between equilibrium states. The choice of the low pulse value is not arbitrary. The low value of the pulse must correspond to a current within the bistable region. Therefore, $I_{in,\text{low}}$ must be selected within the hysteresis loop (see Figure 5.5b).

For this analysis, $I_{in,\text{low}} = 25\,\text{nA}$ was chosen to ensure operation within the bistable region. Figure 5.6 illustrates that, depending on the pulse amplitude, the system stabilizes at one of the two equilibrium states, regardless of the final value of the input



(a) Transient simulation.

(b) Hysteresis loop.

Figure 5.5: Analysis of the bistable circuit. (a) Time evolution of the system under triangular input, showing transitions between states and hysteresis. (b) Hysteresis loop illustrating the system's bistable nature with distinct switching thresholds.

current. This confirms that the system exhibits two stable equilibrium states. Depending on the initial condition, the system remains in one of these equilibria, but if the disturbance is large enough, it transitions to the other equilibrium.

The initial condition in this case is determined by the voltage across the capacitor. In our simulations, this voltage is set to $V_c = 0\,\mathrm{V}$ as initial conditions.

Effect of Initial Conditions

In the previous section, we mentioned that the initial condition influences the equilibrium state. Let us demonstrate this by exploring the sensitivity of the system to initial conditions. By varying the initial voltage across the DPI capacitor , the circuit stabilizes in different equilibrium states for the same I_{in}. This behavior is illustrated in Figure 5.7[1]. In this case, the value of I_{in} remains constant and is chosen as before.

Hysteresis

The bistable circuit exhibits hysteresis, as evidenced by the asymmetric thresholds for transitions between equilibrium states. Figure 5.5b shows the system's response to increasing and decreasing I_{in}. The distinct thresholds ensure stability against small perturbations. The width on the ascending part and on the descending part of the

[1]The labels are rounded to two decimal places, giving the impression that the variation is linear, but this is not the case. The variation in V_c is exponential.

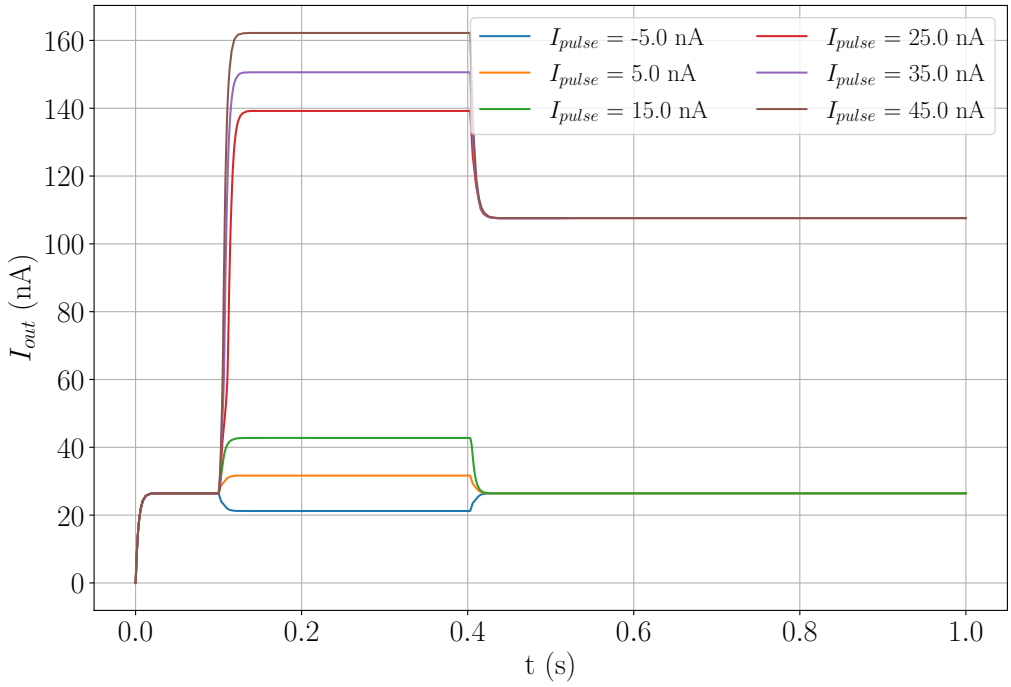


Figure 5.6: Effect of varying input currents on the bistable circuit equilibrium state, with zero capacitor voltage as the initial condition.Pulse amplitude variation is linear.

hystereresis is different because our sigmoid is not symmetrical.

Key circuit parameters

The parameters of this bistable circuit must be chosen carefully. Below, we outline the key parameters, their values, and the rationale behind these choices:

1. **capacitor C of the DPI**: This sets the circuit's time constant and initial condition. A value of 20 pF was chosen to strike a balance: avoiding an overly large time constant that would slow the system's response, while ensuring the circuit is not excessively reactive.

2. **Current I_τ**:
   Together with C, this defines the DPI's time constant. The selected value of $I_\tau = 150$ pA, paired with $C = 20$ pF, ensures a moderate time constant that avoids excessive sluggishness or overreactivity.

3. **DPI gain G**:

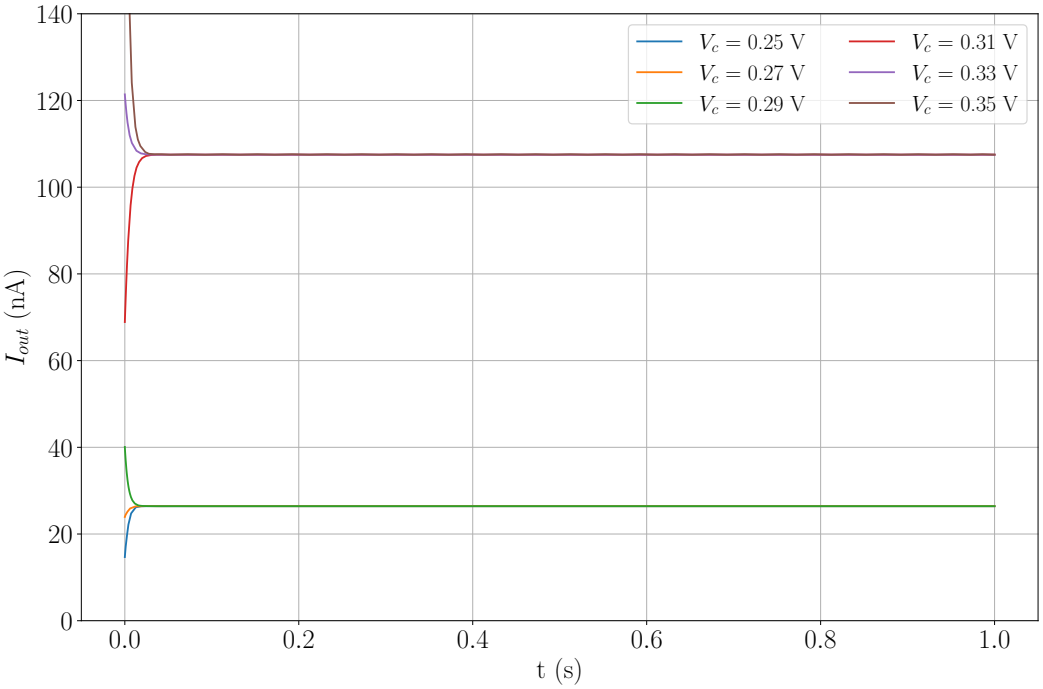


Figure 5.7: Effect of varying initial conditions on the bistable circuit equilibrium state for $I_{in} = 25$ nA. The variation in V_c is exponential.

Set to 1 for simplicity, allowing adjustments to the overall system gain to be made via the sigmoid's gain parameter (I_{gain}), without affecting the DPI's intrinsic dynamics.

4. **Sigmoid parameters (I_0, I_{gain}, I_{lin})**:
   These parameters are the most important to determine in order to observe the desired behavior :

   - I_0: Determines the input current at which the sigmoid starts deviating from zero. A value of $I_0 = 50\,\text{nA}$ shifts the bistability region to higher input currents (i.e., to the right on the hysteresis graph). To shift the region to the left, I_0 can be reduced (see Figure 5.8a).
   - I_{lin}: Specifies the width of the sigmoid's linear region, influencing the smoothness of state transitions. For $I_{lin} = 15\,\text{nA}$, transitions are sharp enough to maintain a distinct hysteresis. Increasing I_{lin} reduces the width of the hysteresis loop, while decreasing I_{lin} accentuates it (see Figure 5.8b). Changes in the hysteresis loop are mostly noticeable on the left branch of the graph. To demonstrate bistability, a sigmoid with a narrow linear region is preferred to ensure operation within the bistable region. A large value of I_{lin} may result in behavior closer to the monostable case, diminishing the bistability.

- I_{gain}: Controls the saturation level of the sigmoid and influences the gap between the two stable states, as well as the overall width of the hysteresis loop (see Figure 5.8c). Like I_{lin}, it affects the slope of the sigmoid. With $I_{gain} = 50\,\text{nA}$, the separation between stable states is sufficient for clear bistability.

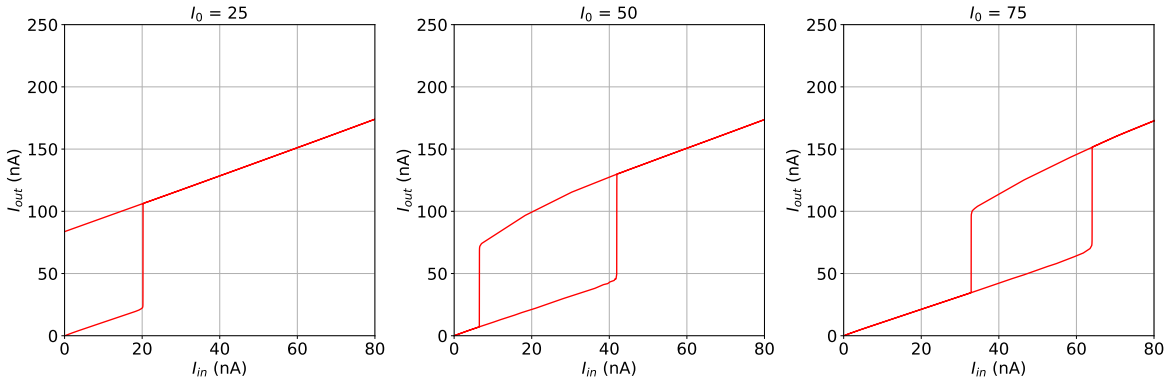
These parameters ($I_0 = 50$ nA, $I_{gain} = 50$ nA, $I_{lin} = 15$ nA) allow us to observe the desired behavior. Alternative values can achieve similar behavior but may require further fine-tuning. The choice of values is not independent of each other; we choose our three parameters in such a way as to achieve the desired behavior. Changing one parameter often requires changing another to achieve the desired result.

5.3.3 Conclusion

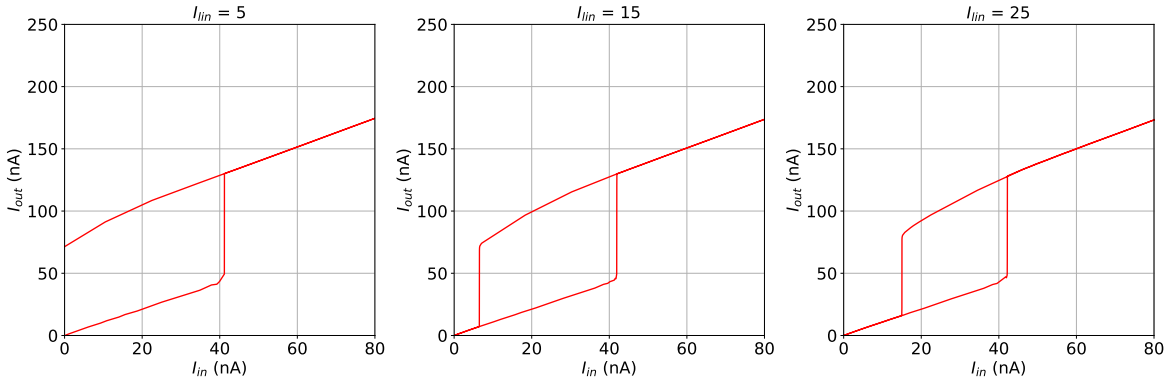
In view of the results, the bistable circuit implemented in *Cadence* is capable of exhibiting nonlinear behaviors, such as bistability and hysteresis, under appropriate conditions. Positive feedback allows the system to stabilize in one of two equilibrium states, depending on the input current I_{in} and the initial voltage configuration of the capacitor. In the bistable region, transitions between equilibrium states only occur when disturbances are large enough to switch between equilibria.

Although minor deviations from theoretical predictions were observed, mainly due to parasitic capacitances and non-ideal transistor characteristics. These deviations did not affect the qualitative behavior of the circuit. In particular, the DPI gain deviates from the expected value for gains other than 1. However, the overall system gain is entirely determined by the sigmoid gain, which simplifies parameter tuning. In our analysis, the precise value of the gain has no significant impact on the overall behavior of the circuit, which remains our main objective.

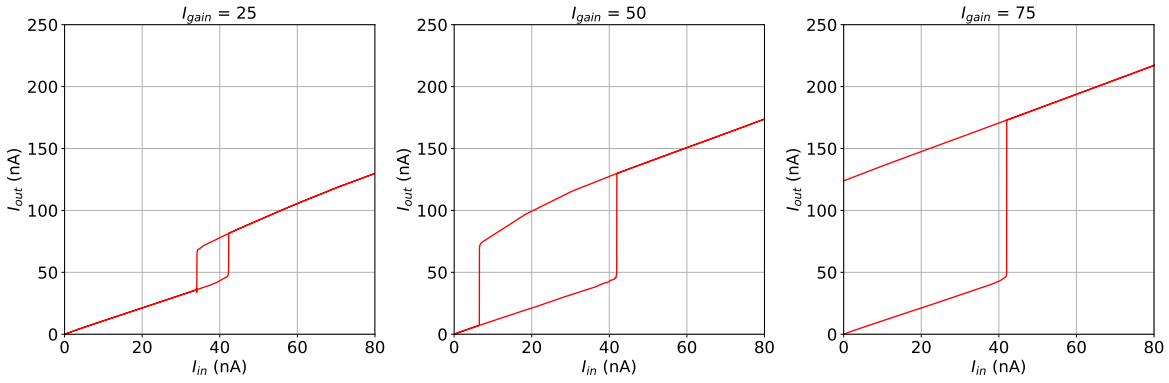
We also observed that the hysteresis loop has asymmetric rising and falling branches due to the asymmetry of the circuit's sigmoid. However, this asymmetry does not significantly impact the system's bistable behavior. Finally, we highlight the importance of carefully selecting the circuit parameters to achieve the desired behavior.



(a) Impact of parameter I_0 on system hysteresis. The hysteresis is shown for three different values of I_0 with $I_{lin} = 15$ nA and $I_{gain} = 50$ nA.



(b) Impact of parameter I_{lin} on system hysteresis. The hysteresis is shown for three different values of I_{lin} with $I_{gain} = 50$ nA and $I_0 = 25$ nA.



(c) Impact of parameter I_{gain} on system hysteresis. The hysteresis is shown for three different values of I_{gain} with $I_{lin} = 15$ nA and $I_0 = 50$ nA.

Figure 5.8: Hysteresis plots showing the impact of varying I_0, I_{gain}, and I_{lin} on the system, while keeping the other parameters constant.

Chapter 6

Fast and Flexible Decision Modeling for CMOS Applications

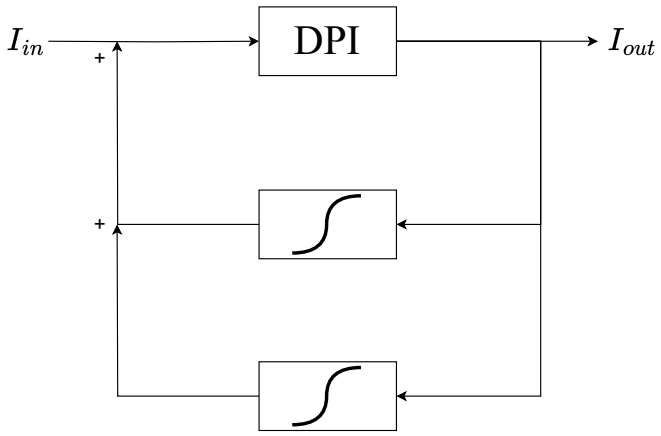


Figure 6.1: Diagram of the fast and flexible decision circuit combining DPI and sigmoid blocks in a positive feedback configuration.

This chapter explores a circuit designed to achieve multistability with 3 equilibrium states by combining a DPI with two sigmoid blocks, each with distinct parameters. The system operates via a positive feedback loop, where the output of the DPI feeds the inputs of the two sigmoid blocks. This configuration, implemented in *Cadence*, enables the circuit to stabilize in one of two or three equilibrium states, depending on the input current I_{in} and the circuit parameters.

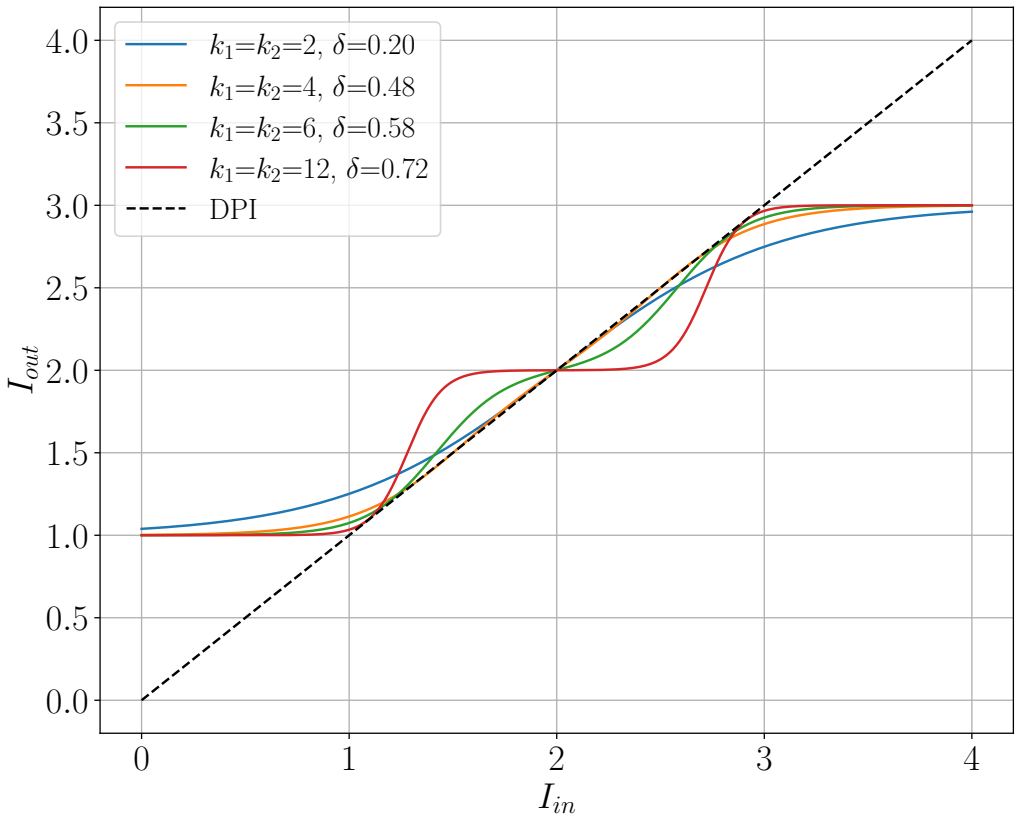


Figure 6.2: Illustration of double sigmoids in the configuration for tristability (see section 4.2.2). The figure shows that if the slope of the sigmoids is equal to or smaller than that of the DPI dynamics, the system does not reach the desired configuration. Additionally, for steeper slopes, a larger gap δ (the distance between the symmetry point and the inflection points of the two sigmoids) is required to achieve tristability.

6.1 Objectives and Experimental Approach

In the theoretical analysis, we varied k to identify the desired point in the bifurcation diagram. The gain allowed us to adjust the relative position of the sigmoid in relation to the dynamics of the DPI, as it also influenced the slope.

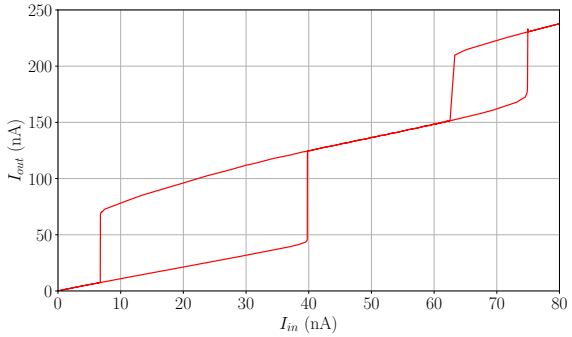
In the circuit design, we selected constant gain and slope values to ensure a relatively steep slope (greater than that of the DPI dynamics[1]). We then introduced a significant initial gap between the two sigmoids and gradually reduced this gap until a tristable region emerged.

The process involves progressively narrowing the distance between the two sigmoids until their alignment matches the theoretical predictions. This approach facilitates an easy transition between double bistability and tristability by adjusting $I_{0,2}$. The steeper the slope of each sigmoid, the larger the required distance between the two sigmoids to achieve tristability. This procedure is illustrated in Figure 6.2 and will be developed further in this chapter.

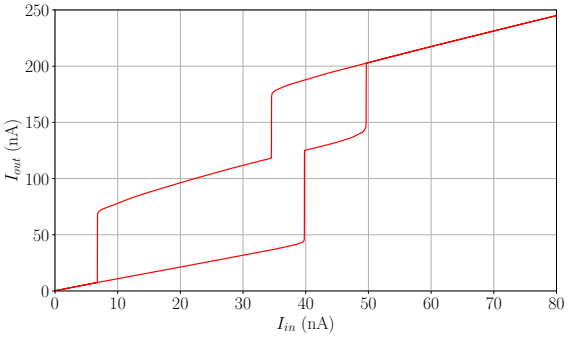
The primary objective of this chapter is to investigate the multistability properties of the double-sigmoid system and to highlight its practical implications. To this end, simulations were conducted in *Cadence* under various conditions:

- **Input current variations** to analyze transitions and multistability behavior in relation to input current.
- **Initial condition variations** to study the sensitivity of equilibrium states.
- **Hysteresis properties** to confirm the robustness of the multistability.

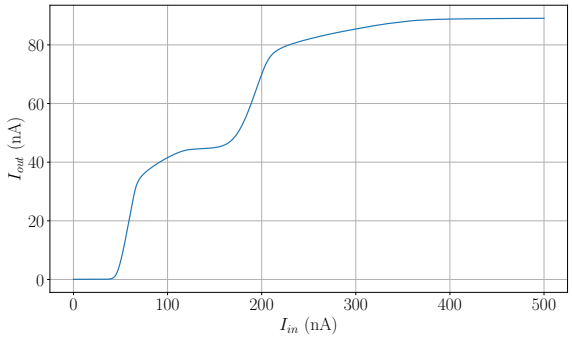
[1] A slope that is too low prevents the observation of the desired behavior. See bifurcation diagram in Chapter 4 and Figure 6.2.



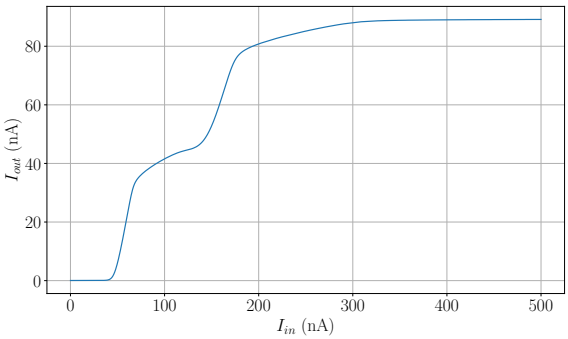
(a) Hysteresis loop of the system in the double bistable configuration.



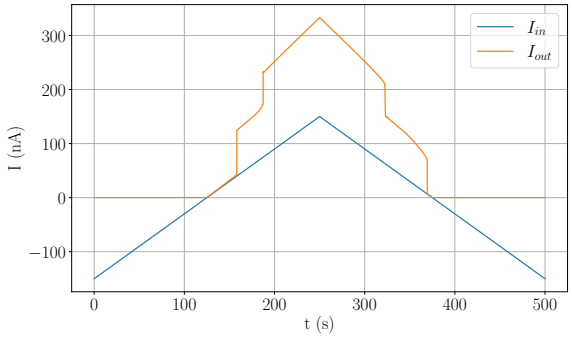
(b) Hysteresis loop of the system in the tristable configuration.



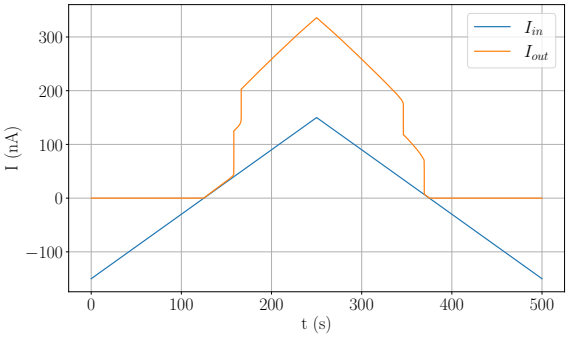
(c) Double sigmoid shape used for double bistability.



(d) Double sigmoid shape used for tristability.



(e) Response of the system to a triangular input signal in the double bistable configuration.



(f) Response of the system to a triangular input signal in the tristable configuration.

Figure 6.3: The figures on the left illustrate various characteristics of the system in the double bistable configuration, while the figures on the right depict the corresponding behaviors in the tristable configuration.

6.2 Results and Discussion

In this section, we will present and discuss the results of the various tests carried out to characterize the circuit's behavior

6.2.1 Behavioral Insights

The system's behavior is strongly influenced by the parameters of the sigmoid blocks. Figures 6.6d and 6.6a illustrate that the system can exhibit either double bistability or tristability. By adjusting the width of the "flat" region between the two sigmoids, the system can transition from one configuration to another, as demonstrated in Figures 6.3c and 6.3d.

This transition can also be seen in the system's response to a triangular input, as shown in Figures 6.3c and 6.3d. In the case of multistability with three equilibrium states, the intermediate region is significantly narrower, as illustrated by the hysteresis loop.

6.2.2 Effect of input current variation

The same procedure as in the previous chapter was applied to the tristable configuration. The double bistability configuration was not explored, as the results are expected to be similar to those obtained for the bistable cell.

We applied the same type of input pulse as before, but chose the baseline pulse value within the tristability region (see Figure 6.6d). For our tests, we selected a value of 37 nA. The initial condition was set by initializing the capacitor initial voltage to zero. Figure 6.4 clearly demonstrates that, depending on the pulse amplitude, the system stabilizes in one of three distinct equilibrium states. These results confirm the existence of three equilibrium states, in line with theoretical predictions.

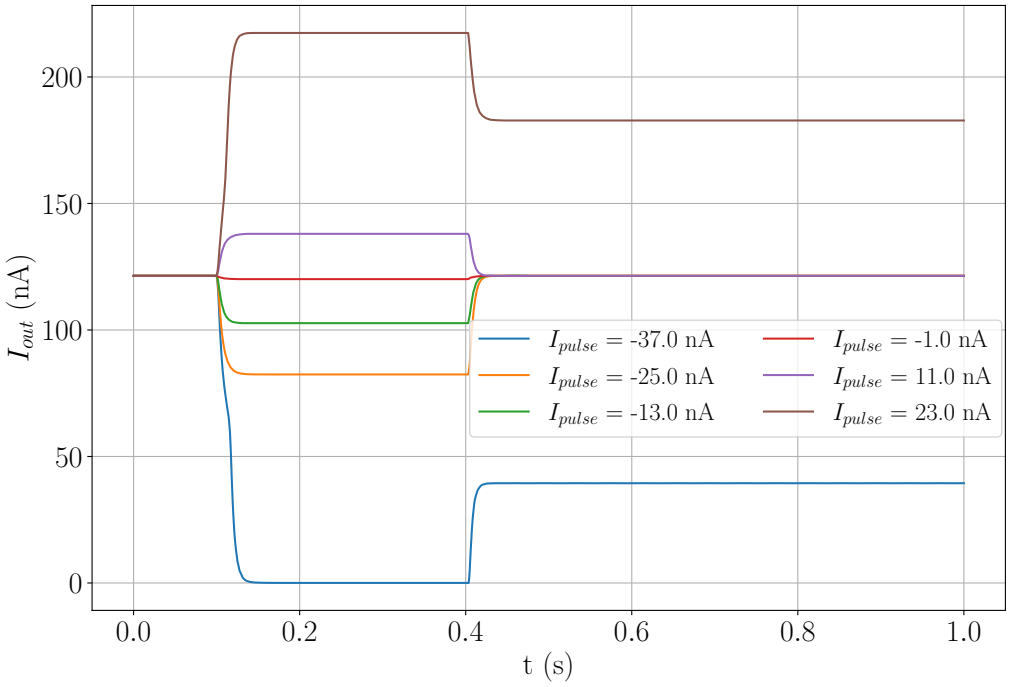


Figure 6.4: Effect of varying input currents on the tristable circuit equilibrium state, with zero capacitor voltage as the initial condition. Pulse amplitude variation is linear.

6.2.3 Effect of Initial Conditions

The influence of initial conditions was further analyzed by varying V_c while maintaining a constant input current within the multistable region. Simulations revealed that different initial values of V_c led to stabilization in one of three distinct equilibrium states (see Figure 6.5). This sensitivity highlights the critical role of initial conditions in determining the system's equilibrium state. All simulations were performed with a constant input current of 37 nA.

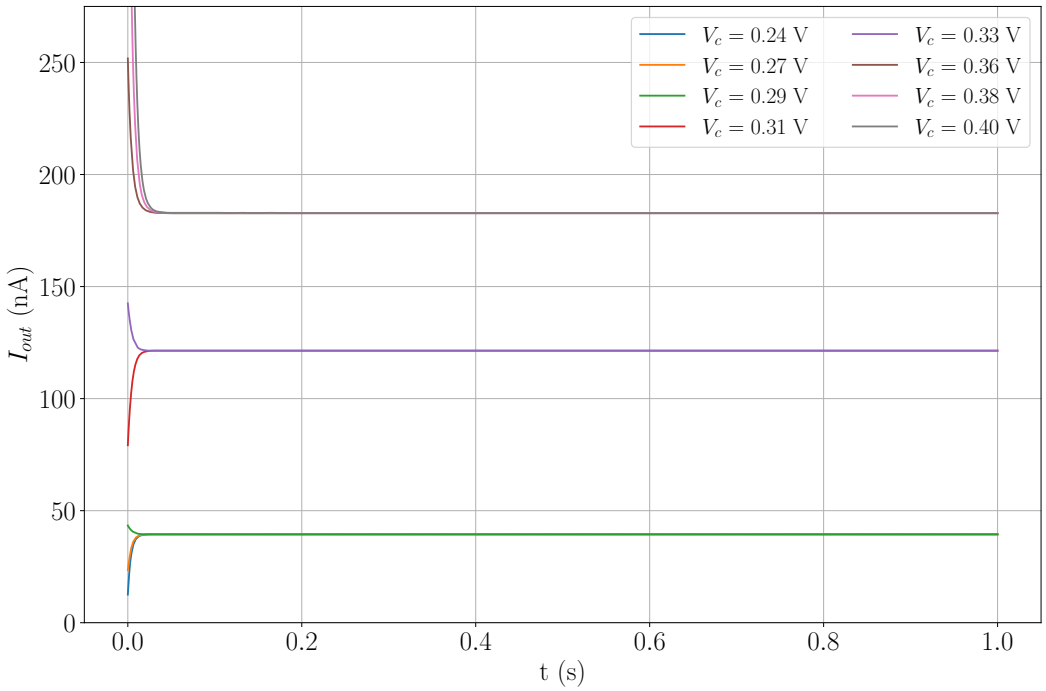


Figure 6.5: Effect of varying initial conditions on the tristable circuit equilibrium state for $I_{in} = 37$ nA. The variation in V_c is exponential.

6.2.4 Key cricuit parameter

The interaction between the two sigmoid blocks introduces an asymmetry in the bistable zones. This asymmetry is due to the fact that the second sigmoid influences the first, thus modifying the overall shape of the feedback loop. This interaction accelerates the saturation of the first sigmoid, creating regions of different sizes, as shown in the following Figures 6.6a and 6.6d.

The results presented here are based on theoretical parameters designed to exhibit the desired behavior: both sigmoids have identical linear regions and the same gain. The only parameter modified is $I_{0,2}$, which determines whether the system operates in a double bistable or tristable configuration. However, this approach reveals certain limitations. Similar to the bistable circuit, rising and falling parts are not always the same size in the hysteresis loop, but that's something we can't change. One major difference, however, is that the circuit introduces two bistable zones of different lengths and widths.

Building on the earlier analysis of parameter impact on hysteresis 5.3.2, we explored whether adjustments to the parameters could mitigate these non-idealities. To address this, we reduced the linear region of the second sigmoid and slightly increased its gain. These adjustments resulted in two bistable zones in the hysteresis graph that are nearly identical. Figures 6.6a and 6.6d illustrate the new hysteresis curves after these modifications, which were designed to counteract the asymmetries inherent in the double sigmoid circuit.

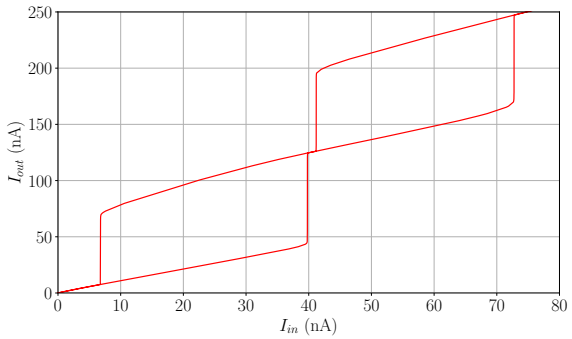
With these new parameters, the bistable and tristable zones align more closely with theoretical predictions. In addition, we can now afford to have a region that can handle a greater number of I_{in} values without changing the overall behavior of the system. The final parameter values are:

- $I_{lin,1} = 15\,\text{nA}$,
- $I_{lin,2} = 3\,\text{nA}$,
- $I_{gain,1} = 25\,\text{nA}$,
- $I_{gain,2} = 30\,\text{nA}$,
- $I_{0,1} = 50\,\text{nA}$.

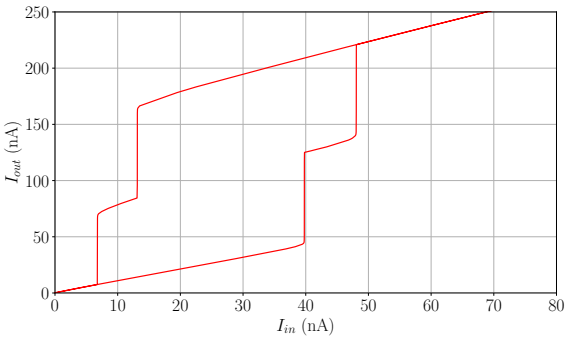
Previously, the same I_{lin} and I_{gain} values were used for both sigmoids. To switch between the double bistable and tristable configurations, only $I_{0,2}$ is modified. Specifically:

- $I_{0,2} = 150\,\text{nA}$ is used for the tristable configuration.
- $I_{0,2} = 180\,\text{nA}$ is used for the double bistable configuration.

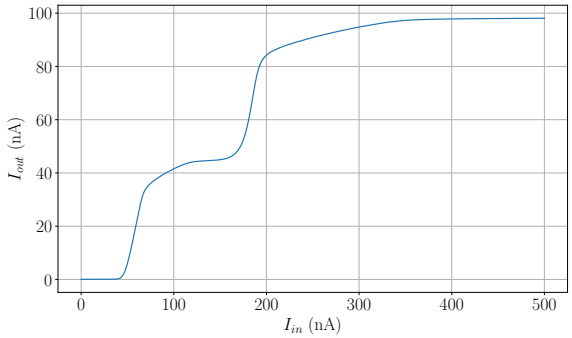
Indices 1 and 2 refer to the first and second sigmoid. The double sigmoid system demonstrates versatile multistability behaviors.



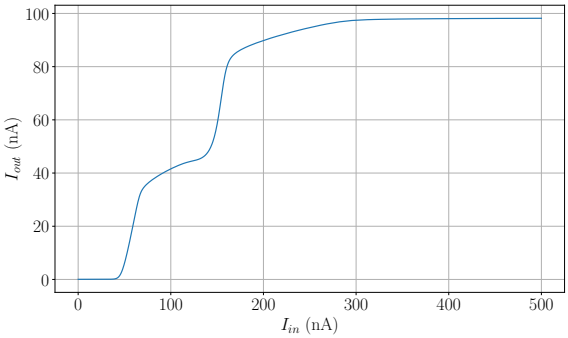
(a) Hysteresis loop of the system in the double bistable configuration.



(b) Hysteresis loop of the system in the tristable configuration.



(c) Adjusted sigmoid for the double bistable configurations



(d) Adjusted sigmoid for the tristable configurations

Figure 6.6: New hysteresis curves and their corresponding double sigmoids after adjusting the parameters of the second sigmoid to counteract the asymmetries in the circuit behavior.

Chapter 7

Conclusion and Future Work

In conclusion, the main objective of this thesis was to design and implement circuits capable of demonstrating multistability and hysteresis, two fundamental phenomena in nonlinear systems. This work explored the underlying theory of these phenomena right through to the design of corresponding neuromorphic circuits.

The project was divided into three key phases. The first part introduced CMOS transistors and their application in neuromorphic circuits, laying the groundwork for the entire study. The second part delved into the theoretical principles of non-linear dynamics, feedback, multistability, and hysteresis, supported by simulations conducted in *Julia* to validate these concepts. The bifurcation analysis in this phase provided key insights into how to identify regions of bistability and tristability. Finally, the third part bridged the gap between theory and practice by implementing these phenomena in actual circuits designed and simulated using the *Cadence Virtuoso* platform.

One of the main achievements of this work was the successful demonstration of bistability and tristability in neuromorphic circuits. By combining a Differential Pair Integrator and one or two sigmoid blocks, we showed how careful parameter tuning could control the number of equilibrium states and achieve complex dynamic behaviors. In particular, the double sigmoid configuration exhibited richer dynamics, including two bistable regions and, with appropriate adjustments, a tristable region. This experimental validation underlines the robustness and adaptability of these circuits.

The circuits implementation in *Cadence Vituoso,* demonstrating that such designs are feasible within realistic technological constraints. Although some non-idealities emerged due to transistor characteristics, most discrepancies could be mitigated through parameter adjustments, confirming the practical viability of the designs.

In the end, this thesis demonstrates that multistability and hysteresis can be effectively exploited to improve the performance and adaptability of neuromorphic circuits. Future work could focus on the design of a physical chip implementing these dynamic behaviors, which would be useful in the development of low-power, adaptive neuromorphic systems.

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