Master thesis : Design, simulation and modeling of a multiport electrical converter for Standalone Building-Integrated Photovoltaic systems

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Master Thesis

Design, simulation and experimental validation of a multiport electrical converter for Standalone Building - Integrated Photovoltaic systems

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Graduation Studies conducted for obtaining the Master's degree in Electrical Engineering by
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Supervised by Fabrice Frébel and Benoît Bidaine

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Abstract

Renewable energies have been growing worldwide in the recent years to avoid environmental degradation. Among the renewable sources, solar energy is regarded as the most promising candidate and is expected to be the foundation of a sustainable energy economy, as sunlight is the most abundant resource. Recently, standalone building integrated photovoltaic systems (SBIPVs) have risen as a solution to reduce the electrical needs of buildings, in which photovoltaic cells are integrated into the construction envelope. The need for further integration between photovoltaic systems and batteries is of paramount importance, requiring an improvement in the energy conversion paradigm.

The development of a three-port bidirectional converter for SBIPVs is the main focus of this project. A review of currently in research topologies is done, selecting the most suitable for the application. A theoretical analysis of the selected topology is performed, with a validation of the computations present in the reference paper. A simulation of the converter circuit is designed to assess its different characteristics and operating range. A design procedure is followed with a choice of the different parameters that will define the converter in order to meet the requirements of the application in hand, with a theoretical and simulation analysis process. A prototype of the designed converter is finally done to experimentally validate its functionality through a testing phase.

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Chapter 1

Introduction

Traditionally, photovoltaic systems and batteries have had independent energy conversion stages. Differences in their electrical behaviour, as well as interaction with control and management systems, made it a more feasible option to treat them as two independent entities that may be working together. Their connection was merely reduced to two systems that could be involved in the same network. As these electrical networks grow larger in size and more elements are interconnected together, the use of one electrical converter per element has become nonviable.

Recently, building integrated photovoltaic systems (BIPVs) have risen as a solution to reduce the electrical needs of buildings. New European regulations have established the need for new buildings to be increasingly more efficient and to push forward in the direction of becoming Zero Energy Buildings (ZEBs). These photovoltaic systems are integrated into the construction envelope, making them inseparable. Moreover, the appearance of the standalone systems (SBIPVs) has pushed the technological requirements far beyond. These systems must be able to meet the electrical consumption of the building without interaction with the public electrical grid.

In SBIPVs, the need for harvesting as much energy as possible is as fundamental as it is the storage of this energy to have a stable source of power. This phenomena has increased the integration between photovoltaic systems and batteries, requiring an improvement in the energy conversion paradigm. The development of three-port converters to merge together photovoltaics, batteries and distribution side is of paramount importance. Moreover, battery system require of bidirectionality in the converter, as they can both act as generator or consumer of energy.

The development of a three-port bidirectional converter for SBIPVs is the main focus of this project. This converter must be able to satisfy the technical requirements of these type of installations while maintaining a high energy density and operability at all moments. Its operation range must be able to meet all the possible energy combination between the three port, relying on their bidirectionality. It must be a simple yet efficient solution for the most demanding applications.

First, a theoretical review of the main concepts will be done. In particular, BIPV systems and bidirectionality converters, with special emphasis on the work performed in CE+T Energrid, the hosting company for this project. An analysis of the different converter topologies found in recent literature will be done, aiming at selecting the most suitable one for the application.

After the selection of the suitable topology introduced on a reference paper, it will be analyzed to assess its functionality. The theoretical computations done in the article will be reviewed and a simulation will be performed to compare them and validate the results presented in the paper.

Next, the design of the converter for the project will be done. The main parameters will be chosen according to the requirements. A theoretical analysis will be done, as well as a simulation analysis with special emphasis on the waveforms obtained during the different operation modes. Further analysis such as voltage range, sensibility and efficiency will also be performed.

A prototype of the converter will be built afterwards. The main parts of the process will be explained into detail, with special emphasis on the magnetic components design and the control programming. The assembling process will be the final phase of the prototyping.

Finally, a testing phase will be initialized, aiming at trying the different operating points and comparing them to both the theoretical computations and the simulations performed. Tests will be divided into control and power tests, in which different parts of the prototype will be validated.

Some conclusions will be drawn afterwards to certify if the designed converter does indeed meet the requested specifications. Final annexes will include information about the hosting company, as well as technical aspects such as a bill of materials, the component ratings, schematics and the microcontroler code.

Chapter 2

Theoretical Background

2.1 Building-Integrated Photovoltaic (BIPV) Systems

Renewable energies have been growing worldwide in the recent years to avoid environmental degradation. Moreover, the implementation of distributed energy generation to be able to electrify rural areas has risen the opportunity to develop new technologies for renewable energy generation, as they are the most commonly accessible in these areas.

Among the renewable sources, solar energy is regarded as the most promising candidate and is expected to be the foundation of a sustainable energy economy, as sunlight is the most abundant resource [1]. Solar energy generation involves the use of sun energy to provide hot water or electricity. In the case of solar photovoltaic (PV), the system directly converts solar energy into electricity.

Using PV stations to produce electricity has proven to be one of the most sustainable methods. Its advantages are various, including no atmospheric emissions or radioactive waste generation during use; reduction on the dependence and pressure on the central utility lines in systems with high potential for blackouts and overloads as it acts as a distributed electrical generation source; assistance in national energy security and long-term economic growth improvement for any country developing the technology [2].

It is assumed that future massive photovoltaic applications will involve mainly urban areas, as more than 80% of inhabitants of the most developed countries live in these environments [3]. Before establishing a photovoltaic system in an urban environment, it is important to assess the solar potential of the area, which depends directly on the local exposure to sunlight. Irradiation variation, which happens locally, arises the need to fabricate modeling tools that take all possible factors into account [4].

When using PV systems on buildings, two main types can be distinguished: building attached (BAPV) and building integrated (BIPV). The differentiation, even though clear from a theoretical point of view, can sometimes be diffuse if the mounting method of the system is not clearly stated [5]. BAPVs generally represent the systems that are not attached to the structure and therefore do not have a direct effect on its function. They are mainly additions to the building.

BIPV systems are defined as photovoltaic modules that can be integrated in the building envelope (roof or façade) by replacing conventional building materials [6]. The difference with BAPV is therefore clear, as it has an impact on the structure functionality of the building. They are directly integrated on the energy system of the building.

Usually, existing BIPV capability or potential is reviewed in an either geographically-limited or functionality-limited fashion. It is necessary to move on from this vision and to be able to establish a valid model that would represent a viable project for all buildings, without undermining the special characteristic that each project must have. On that note, new European legislation is being pushed forward on this direction.

The European legislation package known as 'Europe 2020' included different targets aiming at fighting against climate change. The main objectives where to cut in 20% greenhouse gas emissions compared to the 1990 levels, obtain 20% of the EU energy from renewable sources and obtain a 20% improvement in energy efficiency [7]. Moreover, new targets for 2030 have been recently established, rising the target to 40% reduction of greenhouse gas emissions, 27% of renewable share and 27% of improvement in energy efficiency [8].

To be able to achieve these objectives, it is necessary to implement what is known as Zero Energy Buildings (ZEBs or NZEBs). These types of buildings are able to generate the energy needed to meet the demand of the building by themselves. To do so, it is important to exploit all the PV potential of the building, including both roof and façade. In a modern city, the available area on vertical walls (façades) far exceeds the buildings' roofs. Recently the trend has turned to the development of methodologies for the analysis of the solar assessment of façades [9].

Moreover, other renewable sources can be also used on buildings to improve its energy generation and efficiency (mainly thermal power, with BIPV/T, and wind power, with micro turbines). BIPV/T systems use both PV and thermal energy to improve the efficiency. Usually, air flows through the façade to take out the heat and improve the system efficiency and lifetime. However, in this type of installations the heat produced at the PV panel is used to reduce the heating load of the room, with a fan and an air duct to insert the air flow inside. This system method is still far more expensive than the regular BIPV [6].

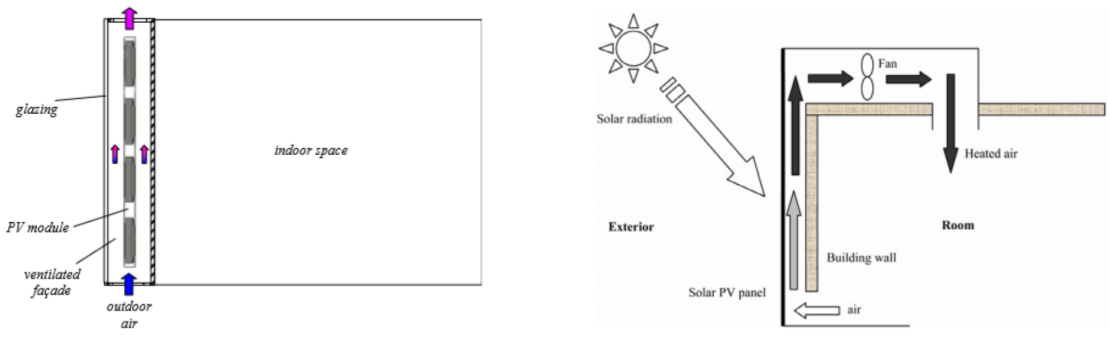

Figure 2.1: BIPV façade system [10] and BIPV/T façade system [11], respectively.

The choice between BAPV and BIPV systems for existing buildings does not have a unique solution and depends on different criteria. While BIPV's level of integration is particularly high as the PV arrays can act as building envelopes, such as curtain walls or windows, their total cost is considerably higher when compared to BAPV systems. The latter have also the main benefit that their malfunction does not affect the structure of the building and it is not therefore a critical issue [12].

The key factors to BIPV development are low production cost, low environmental impacts and high efficiency. On the former, it is crucial to have a relatively easy installation method for existing buildings. To be able to penetrate the market in a worldwide scale, these systems must not be exclusively built for new buildings as it would not be sufficient to meet the European environmental objectives [13].

Many parameters must be taken into account when assessing the feasibility of an installation. On the one hand technical aspects such as design, durability, performance and maintenance are of clear importance. On the other hand, aesthetics and buildability are also essential to be able to sell the product, as well as other aspects like safety, regulations and environmental issues. All in all, the installation must be done in the best way possible to ensure it properly fits its purpose [6].

Generally, PV systems can be classified in two groups: off-grid and grid-connected. A grid-connected system uses an inverter to convert electricity to AC to be then supplied to the electrical grid. They can be either distributed, if the system is connected to a particular customer or network, or centralized, if it works as a power station without any association to any individual. The costs are generally far lower than in the off-grid case as they do not require an energy system [14].

Off-grid PV systems, also known as Standalone systems, have a significant opportunity for economic application in the unelectrified areas of developing countries. Moreover, as technology evolves and energy efficiency drastically improves, they can become a reliable option for networks that do not want to depend on the grid or that simply want to create their own community microgrid. Due to the intermittent nature of renewable sources (solar power among them), an energy storage system is of paramount importance to be able to meet demand with deisregard of the time of the day or year it is. The main objective would be to store energy at peak hours when the generation overcomes demand to be able to use that same energy at valley hours, when generation is not able to meet demand.

BIPV systems still represent a small share of the PV market due to the perception of them being far more expensive and less reliable than conventional roof installations. It is therefore vital to be able to penetrate the market with a straight-forward product that can meet the main demands from the building sector. Even though they have been extensively studied in the recent years, there is still a need to further improve its efficiency. The development and increased popularity of ZEBs will open a niche market for BIPVs, as they will be essential to achieve new standards and pollutant emission objectives.

2.2 Bidirectional Energy Conversion

Since the discovery of electricity, there has been a need to manipulate its parameters at will rather than having to adapt consumption to generation. Converters allow different types of generation and consumption systems to be interconnected even if their characteristics radically differ.

Traditionally, converters have been designed specifically to allow power flow from the generation to the load side. The increase in energy density and the reduction in price of batteries has popularized their use on the electrical system as back-up solutions and to complement the local energy production. Due to the hybrid nature of energy storage systems, which can either work as generation or consumption, there is a growing need to rethink traditional unidirectional converters.

Nowadays, the energy management system scheme is becoming essential on every local energy system. The need for bidirectional converters to operate and control this energy management is therefore crucial. Indeed, bidirectional converters allow systems to control power flows among all connected sources to optimize the load supply at desired criteria. The interoperability among different converters allows to connect far more distributed and complex systems [15].

Direct current is also being rediscovered following the rise of renewable energy sources and energy storage. Moreover, DC/DC conversion allows for a more efficient and simpler operation than AC/DC as it does not involve resynchronization [15]. New designs and conversion methodologies are being explored to further improve DC/DC conversion operation. Its limit has not been reached and there is still room for improvement.

As grids grow exponentially in complexity and more and more elements have to be interconnected, conversion stages become far too numerous to handle properly in local systems. A need to reduce and simplify conversion stages and functionality is clearly foreseen. The availability of a suitable multiport DC-DC converter is therefore of paramount importance. High efficiency, modularity, low components count and ease of control are some of the main features that these types of converters must have to interface with renewable sources, loads and storage elements [16].

Along with the new paradigm of bidirectional, multiport energy conversion, a need to feature new control scheme arises. Indeed, the system must be easily manageable and able to be customized at maximum, more so from the end user point of view. Different control strategies can be explored, either linked to internal variables such as source availability or consumption, or to external characteristics, such as market price or weather conditions.

Power conversion is becoming increasingly essential in any system, no matter its size or its location. Differents paths for research are currently available, as it has been briefly introduced in this section. Bidirectional multiport converters will be the main focus during the following chapters, with the review and design of a converter topology that will try to meet all the criteria explored in this section.

2.2.1 Development on CE+T

CE+T (*Constructions Electroniques + Telecommunications*) is a Belgian-based company specialized in backup power solutions. Its main range of products can be categorized into inverters, UPS and converters. A more detailed overview of the company can be found in the Annex. In this section, an analysis of the bidirectional converters developed in the company will be done, with special interest in its technology and uses.

The main technology developed and currently being used in the newest converters of the company is the ECI (Enhanced Conversion Innovation). This technology combines three patented ports, two AC and one DC. One of its main features is a 0-ms transfer time between AC and DC input. This allows to switch inputs when one of them fails or is not available without any interruption on the system.

The ECI technology combines three energy converters (two AC/DC for the AC ports and one DC/DC for the DC port) and an energy buffer. The efficiency of the converters is of 96% in the AC/AC transfer and of 94% in the DC/AC stage. In particular, the DC/DC converter built on the DC port allows efficiency greater than 98% [15]. On Figure 2.2, the ECI schematics is displayed, with details of the AC/DC stage and DC/DC converter.

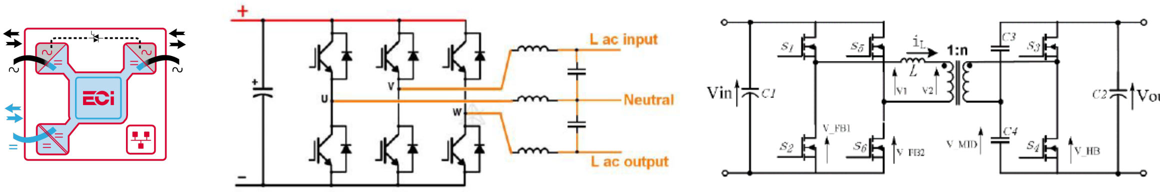

Figure 2.2: ECI technology (left), AC/DC (middle) and DC/DC (right) stage [15].

Bidirectionality is possible in all ports. This feature allows the converter to be used as power routers, mixing power from different sources (such as AC grid, battery and renewable sources) and connecting it to different loads, either AC or DC. Therefore, ECI converters can be used for many purposes, such as peak shaving, phase-balancing, battery management and energy restitution.

CE+T is currently developing its own family of bidirectional converters by means of the ECI technology under the name Sierra. The first module available is the Sierra 25, which can provide up to 2,4 kW on any port. The module is designed at a voltage rating of 48 Vdc and 230 Vac. It can be used for single-phase or three-phase operation at either 50 or 60 Hz.

Several modules can be synchronized to get large systems of up to 32 modules (allowing for a maximum of 75 kW of power per system). Each module has its own controller without any master/slave system, which allows the system to continue operating even if a module fails. Reliability is therefore one of the key features of the converter and an important objective of all the products from the company.

2.3 Converter Topologies

Renewable energies are fast gaining their position as the preferred generation method worldwide. However, their intermittent nature is still one of the main drawbacks of these technologies. It is therefore essential to have a storage device to save the energy produced at peak hours to be later used when generation is not sufficient to satisfy the demand.

Traditionally, a two-step conversion has been used, in which the renewable source and the load where connected through a DC-DC converter and the energy storage was connected to either the source or the load through a bidirectional DC-DC converter. This yields a system with lower efficiency and power density and potentially increased size and cost [17].

As opposed to this, the three-port DC-DC converter has gained popularity in the recent years. It eliminates the need to have two converters by adding an additional input in which the device storage can be connected. The additional port must be bidirectional to satisfy the charging and discharging requirements of the storage device. There are three main types of three-port converters depending on its isolation.

A non-isolated converter has all its ports sharing the same power ground with no transformer in between. It has the benefit of having less components and, therefore, a reduced size. However, its voltage gain is limited as it often relies in traditional buck-/boost converters. Even though adding inductors could solve this problem, this would imply the loss of the reduced size and cost, which was its main advantage [18].

Partly-isolated controllers are an intermediate solution when some port needs to be isolated. Two of the ports share the same power ground while the third is isolated through a simple transformer. It is generally still a simple structure, even though its reliability is lower than in the non-isolated type . It allows for higher customization of the voltage levels of the isolated ports while still having two similar ports sharing a single structure [19].

When galvanic isolation is mandatory for all ports, an isolated converter is to be used. All ports have independent reference potential and the energy transfer is combined into a single magnetic device. They are generally more complex designs in which magnetic characteristics, such as leakage inductance caused by imperfect coupling, can be used for delivering energy transfer, resulting in higher power densities [20].

Non-isolated converters are the most reliable as less switches are usually used. It is preferable for small power applications. Partly-isolated converters allow to control the voltage gain through the transformer ratio but at the expense of a lower reliability. Isolated converters do offer higher customization options in voltage levels but require a larger number of components and the power losses through the leakage inductance of the transformer are higher [17].

For the development of the proposed converter, the isolation is mandatory at all ports. Indeed, PV panels require isolation for polarization, while the DC distribution port requires it mainly for security reasons. Therefore, a fully-isolated converter has to be chosen.

After the analysis of the isolated converters proposed in [17], three interesting configurations have been highlighted. They can be identified by the technology in use: half-bridge, full-bridge or Cuk converter. They will be briefly described to find the most suitable one for the desired application.

The half-bridge topology presented in [21] introduces a bidirectional three-port DC converter. The energy storage is represented by a supercapacitor in one of the ports, which also introduces a boost stage in order to have a wide operating voltage range. A two-level control is included, with variation of the phase shift between bridges and its duty cycle to regulate the power flow and the voltage at the boosted port, respectively.

The main interests of this approach relating to the projected converter is the similarities existant in the load side of the converter, both in voltage and in power levels. Moreover, the converter operates without switching losses under ZVS mode and includes a central power flow control. However, the second control stage is of no particular interest for the scope of this project.

The Cuk topology is introduced in [16]. The author presents a three-port DC converter with one unidirectional port, aimed at connecting an energy source, and two bidirectional ports, for an energy storage system and a grid-tied distribution. An interesting feature is that it does not require any output filter as the ports have a zero-ripple current, characteristic of the Cuk converter. Its simple structure is also of interest, using only three power switches.

The main drawbacks of this topology is the reduced efficiency compared to the bridge topology as no soft-switching occurs. A control system is not included in the paper as the analysis is more focused on magnetics rather than operation range. It is also presented as a new converter which has not been broadly studied, which could induce some problems during the design process. Nevertheless, it is an interesting converter that could be the best choice for applications in which simplicity is highly esteemed and high efficiency is not crucial.

Finally, the full-bridge topology is introduced in [22]. The converter presented on it has been the reference chosen for this project. It will be further developed and its main features explained in the following sections.

Chapter 3

Reference Paper Verification

3.1 Topology Analysis

In the analyzed paper [22], a three-port bidirectional series-resonant converter operating at constant switching frequency is presented. The design introduces different characteristics that define its functionality. All three ports are bidirectional, that is, power can flow both in and out each port. As explained before, it is a crucial feature to have in a renewable source converter, as it must include an energy storage system. It is used differently on each port.

On the first port, dedicated to a renewable energy source generator, bidirectionality is not used as power is always generated and not consumed. On the second port, where an energy storage system is to be connected, bidirectionality is mandatory to be able to both charge and discharge the system depending on the operating conditions. The third port, thought for a load connection, has in bidirectionality an interesting extra feature, as it would allow to connect a load with regenerative capabilities as, for example, a motor with regenerative load.

The power flow control is done by phase shifting the square wave outputs of the three bridges. The MOSFET switches of the bridges are set on or off according to the voltage difference between its gate and its drain. This modifies the output signal of their terminals: when the switch is switched on, current flows through it, and when it is turned off, no current flows and a voltage difference is created between the source and the drain. Using a periodic control signal, a square voltage signal is created. Phase-shifting the bridges implies that the square outputs will be delayed between the different port and, consequently, a power flow will be created among them.

All operating points of the converter and, therefore, all the power flow direction possibilities can be achieved by controlling these phase shifts. Within each bridge, duty cycle is fixed at 50% and no phase shift or delay is introduced inside each bridge. The relation between the phase shift of the different ports and power flows will be further explored in detail in the next chapters.

Figure 3.1 represents the circuit schematics introduced in the reference paper. Port 1 is represented by a constant source of voltage V_1 and injecting a current I_1. A filtering capacitor C_{f1} is added to the source to filter out any oscillations the signal may have. The filtered current i_{1lf} enters the full-bridge, where the four MOSFETs are included. The output current i_{L1} passes through the first resonant tank (C_1 and L_1) and goes into the transformer winding before returning to the full bridge. The square voltage generated by the bridge is represented as V_{1hf}.

Port 2 has an almost equal distribution as port 1. The source is repsented by a battery that can either inject or recieve the current I_2 at a voltage level V_2. After the filter C_{f2}, the filtered current i_{2lf} enters the full bridge and leaves to the resonant tank (i_{L2} entering $C2$ and $L2$) and the transformer winding, returning thereafter to the bridge. If the port is consuming, the opposite direction of currents would occur (and i_{2lf} would be the unfiltered current, consequently). The square voltage at the bridge terminals is represented as v_{2hf}.

Port 3 is set as the load port. Therefore, current is flowing from the transformer windings (i_{ohf} and, respectively, v_{ohf}) to the full bridge, in which the resulting current i_{olf} is filtered through the output capacitor C_o. The port is represented as a resistive load R, with current I_o and voltage level V_o. The transformer is a three-winding transformer, with the ratios being $n_{13}:1$ for port 1 and $n_{23}:1$ for port 2, referenced both to port 3.

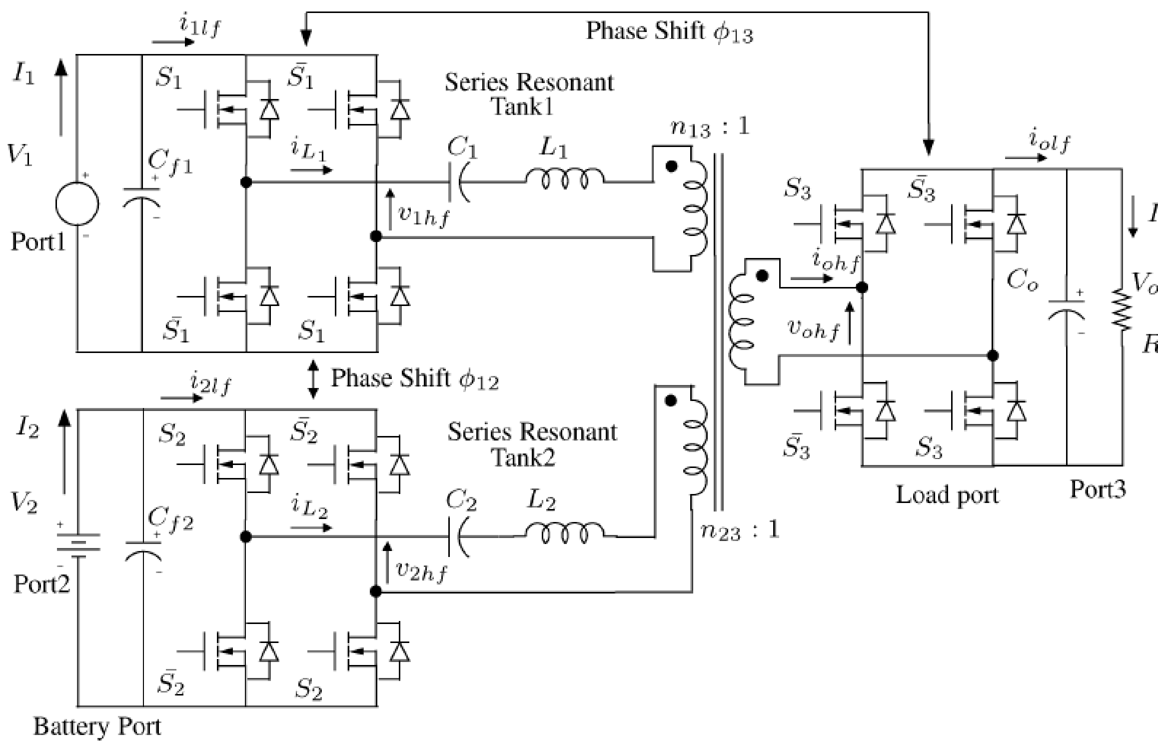

Figure 3.1: Schematics of the converter topology in [22].

The introduction of two series-resonant LC tanks allows for the design to have more freedom in choosing realizable inductance values and switching frequency without dependency. Resonant LC tanks are basically networks whose voltage and current waveforms vary sinusoidally during one or more intervals of each switching period [23]. If no tank would be present, the switching frequency would have to be reduced to get inductance values equal or larger than the leakage inductance of the transformer. Therefore, the resonant circuit allows the converter to operate at higher switching frequencies.

The series resonant circuits also allow the converter to work under reduced losses. Indeed, when the switching frequency of the power bridges is higher than the resonant tank frequency, the converter works under ZVS (zero-voltage switching) conditions (soft-switching operation). If the inverse relationship between frequencies occurred, ZCS (zero-current switching) conditions would occur. However, for power MOSFETs, ZVS is preferred [24].

To ensure ZVS operation, an analysis of the square voltages and currents applied at the resonant tanks of port 1 and 2 can be done. Particularly, if the applied currents lag the square voltages, it ensures that the bridges are operating under ZVS conditions. Regarding port 3, based on the current definition shown in Figure 3.1, the condition changes to leading current for ZVS. All 3 ports will be tested both in simulation and experimentally to certify that ZVS is indeed occuring in all ports at all operating points.

Soft-switching is desired for all ports under all operating conditions. Therefore, some conditions must be met. These will be further analyzed in the following section, in which the converter parameters are computed based, among others, on this requirement. Particularly, as it has been already mentioned, the switching frequency will have to be above the resonant frequency. As parameter computations will be based on the established port voltages, it will also be a condition to maintain the voltage level. If voltage range of the ports changes, ZVS operation may not be ensured, most of all if voltage is below the designed level. Detailed analysis of this phenomena will be addressed in following sections, regarding the voltage range of the converter.

3.2 Reference Design Analysis

An analysis on the design introduced in the reference paper [22] will be first done to assess the accuracy of its computations and validate it. Therefore, the same parameters as the ones in use on the paper will be set. First, a theoretical analysis will be done, aiming at understanding how the converter behaves and computing the different phase shift configurations available. Secondly, a simulation of the converter will be done to completely validate the results introduced in the reference paper and computed theoretically.

3.2.1 Theoretical Analysis

The voltage levels are set at 50 V for port 1 (simulating a renewable energy source), 36 V for port 2 (simulating an energy storage system) and 200 V for port 3 (simulating a load and, therefore, also referred as output port). After setting the port voltages, the turn ratios for the different windings of the transformer can be obtained. In particular, port 3 will be taken as the reference, and ratios n_{13} and n_{23} will be defined:

$$n_{13} = \frac{V_1}{V_3} = \frac{50\ V}{200\ V} = 0.25 \tag{3.1}$$

$$n_{23} = \frac{V_2}{V_3} = \frac{36\ V}{200\ V} = 0.18 \tag{3.2}$$

The converter is rated at a maximum power of 500W. Having the voltage level fixed, the equivalent resistance that corresponds to the defined maximum power can be computed as follows:

$$P_3 = V_3 \cdot I_3 = \frac{V_3^2}{R_o} \quad \rightarrow \quad Z_o = \frac{V_3^2}{P_3} = \frac{(200\ V)^2}{500\ W} = 80\ \Omega \tag{3.3}$$

To compute the values of the inductance and capacitance that form the series resonant tanks, two main conditions are set. It will be of key importance to maintain the resonant tank parameters at both simulation and, further in the process, the experimental validation of the designed converter. An analysis of the sensibility of the design to a change in the tank parameters will be also assessed in another section.

Firstly, the ratio of switching to resonant frequency must be above one for both tanks, that is, the switching frequency must be above the resonant frequency, as has been previously stated in the topology analysis. If this condition is ensured, bridges will operate under ZVS. Taking into account this ratio, the frequency of the resonant tank can be expressed as follows:

$$\omega_i = \frac{1}{\sqrt{L_i \cdot C_i}} = \frac{\omega_s}{F_i} = \frac{2 \cdot \pi \cdot f_s}{F_i} \tag{3.4}$$

where ω_i is the angular frequency of the resonant tank at port i (i=1 or 2), L_i and C_i are the values of the inductance and capacitance, respectively, of the resonant tank at port i, ω_s is the angular switching frequency, F_i is the ratio of switching to resonant frequency of port i and f_s is the switching frequency.

Secondly, the quality factors at each port will be assessed. Its formula is the following:

$$Q_i = \frac{\sqrt{\frac{L_i}{C_i}}}{\left(\frac{8}{\pi^2}\right) \cdot Z_o \cdot n_{i3}^2} \tag{3.5}$$

where Q_i is the quality factor at port i, Z_o is the load port impedance and n_{i3} is the transformer turn ratio between port i and port 3 (load port).

The ratio will be taken as F_i=1,1 for both ports. The quality factors at maximum load (referring to the load that represents the maximum power) will be set at 4,0 so that the sinusoidal approximation is valid [22]. The only unknown values are therefore the resonant tank parameters, which can be obtained for ports 1 and 2:

$$\begin{cases} \dfrac{1}{\sqrt{L_i \cdot C_i}} = \dfrac{2 \cdot \pi \cdot 100\ kHz}{1.1} = 571198\ \dfrac{rad}{s} \\ \\ \dfrac{\sqrt{\frac{L_i}{C_i}}}{\left(\frac{8}{\pi^2}\right) \cdot 80\ \Omega \cdot n_{i3}^2} = 4 \end{cases} \tag{3.6}$$

Given that the turn ratio n_{i3}, where i is either port 1 or 2, is established as $n_{13} = 0.25$ and $n_{23} = 0.18$, the resonant tank parameters and its impedances are the following:

$$\begin{aligned} L_1 &= 28.4\ \mu H & L_2 &= 14.7\ \mu H \\ C_1 &= 0.10\ \mu F & C_2 &= 0.21\ \mu F \end{aligned} \tag{3.7}$$

$$
\begin{aligned}
Z_1 &= \sqrt{\frac{L_1}{C_1}} = \sqrt{\frac{28.4\ \mu H}{0.1\ \mu F}} = 16.85\ \Omega \\
Z_2 &= \sqrt{\frac{L_2}{C_2}} = \sqrt{\frac{14.7\ \mu H}{0.21\ \mu F}} = 8.37\ \Omega
\end{aligned} \tag{3.8}
$$

Once all the parameters of the design are established, the expressions regarding the currents at each port and the power levels both at each port and flowing through ports can be assessed. In figure 3.2, an ideal full-bridge switch is represented, with the voltage and current graphs represented. The output voltage and average current of a controlled full-bridge switch model, according to the references in the figure, can be expressed as:

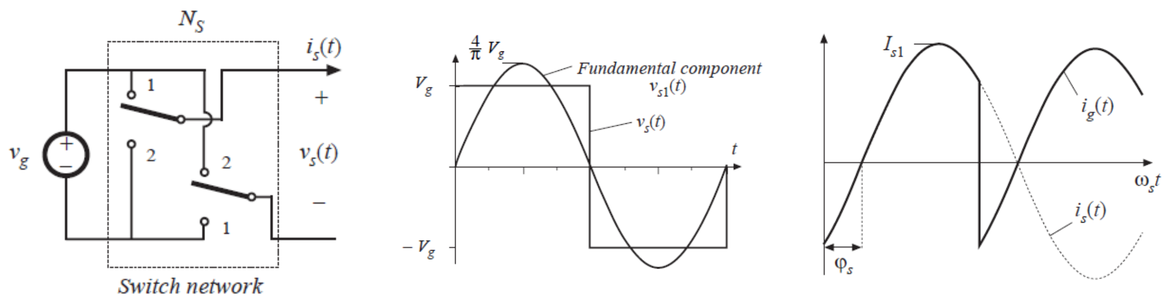

Figure 3.2: Full-bridge switching model with the voltage and current graphs.

$$
v_o(t) = \frac{4}{\pi} \cdot V_g \cdot \sin(\omega_s \cdot t) \tag{3.9}
$$

$$
\langle i_g(t) \rangle_{Ts} = \frac{2}{\pi} \cdot I_s \cdot \cos(\phi_s) \tag{3.10}
$$

Applying the expressions to the analyzed converter, the output current at port 3 can be expressed as:

$$
I_3 = \frac{2}{\pi} \hat{I}_3 \cos(\phi_{13} - \theta_3) \tag{3.11}
$$

where I_3 is the output current at port 3 (current flowing through the load), $\hat{I}_3$ is the peak of the transformer winding current at port 3, ϕ_{13} is the phase shift between ports 1 and 3 and θ_3 is the angle of the transformer winding current at port 3.

The peak of the transformer winding current at port 3 can be also expressed, following phasor analysis, as shown, and substituting it into the output current expression:

$$\hat{I}_3\underline{/\theta_3} = n_{13} \cdot \hat{I}_{L1}\underline{/\theta_1} + n_{23} \cdot \hat{I}_{L2}\underline{/\theta_2} \tag{3.12}$$

$$I_3 = \frac{8}{\pi^2} \cdot \frac{n_{13}V_1}{Z_1\left(F_1 - {}^1\!/\!{}_{F_1}\right)} \cdot \sin\phi_{13} + \frac{8}{\pi^2} \cdot \frac{n_{23}V_2}{Z_2\left(F_2 - {}^1\!/\!{}_{F_2}\right)} \cdot \sin\left(\phi_{13} - \phi_{12}\right) \tag{3.13}$$

where Z_1 and Z_2 are the previously computed tank impedances and F_1 and F_2 are the ratio of switching to resonant frequency, established as 1.1 for both tanks as previously mentioned.

Similarly, the output voltage at port 3 can be expressed as:

$$V_3 = \frac{{}^{V_1}\!/\!{}_{n_{13}}}{Q_1\left(F_1 - {}^1\!/\!{}_{F_1}\right)} \cdot \sin\phi_{13} + \frac{{}^{V_2}\!/\!{}_{n_{23}}}{Q_2\left(F_2 - {}^1\!/\!{}_{F_2}\right)} \cdot \sin\left(\phi_{13} - \phi_{12}\right) \tag{3.14}$$

The values of input (respectively, output) current at ports 1 and 2 can be expressed in similar terms:

$$I_1 = \frac{8}{\pi^2} \cdot \frac{n_{13}V_o}{Z_1\left(F_1 - {}^1\!/\!{}_{F_1}\right)} \cdot \sin\phi_{13} \tag{3.15}$$

$$I_2 = \frac{8}{\pi^2} \cdot \frac{n_{23}V_o}{Z_2\left(F_2 - {}^1\!/\!{}_{F_2}\right)} \cdot \sin\left(\phi_{13} - \phi_{12}\right) \tag{3.16}$$

The dependence of the current to the different parameters can be established from the expressions. In particular, if the voltage port levels are fixed, the current only depends on the phase shift between the ports and, therefore, the power transfer also only depends on it.

Moreover, the current flowing through port 1 only depends on the phase shift between the port and the load port, while the current in port 2 only depends on the phase shift between the port and port 3 (as the two assessed phase shift are the ones between ports 1-3 and 1-2, it is expressed as the difference between them). This phenomena will be further explained in the next sections.

The currents at all ports can be expressed as, including the values of all known parameters:

$$\begin{aligned} I_1 &= \frac{8}{\pi^2} \cdot \frac{n_{13} \cdot V_o}{Z_1 \cdot (F_1 - {}^1/_{F_1})} \cdot \sin\phi_{13} = \\ &= \frac{8}{\pi^2} \cdot \frac{0.25 \cdot 200}{16.85 \cdot (1.1 - ({}^1/_{1.1}))} \cdot \sin\phi_{13} = 12.60 \cdot \sin\phi_{13} \end{aligned} \tag{3.17}$$

$$\begin{aligned} I_2 &= \frac{8}{\pi^2} \cdot \frac{n_{23} \cdot V_o}{Z_2 \cdot (F_2 - ({}^1/_{F_2}))} \cdot \sin(\phi_{13} - \phi_{12}) = \\ &= \frac{8}{\pi^2} \cdot \frac{0.18 \cdot 200}{8.37 \cdot (1.1 - ({}^1/_{1.1}))} \cdot \sin(\phi_{13} - \phi_{12}) = 18.26 \cdot \sin(\phi_{13} - \phi_{12}) \end{aligned} \tag{3.18}$$

$$I_3 = n_{13} \cdot I_1 + n_{23} \cdot I_2 = 0.25 \cdot I_1 + 0.18 \cdot I_2 = 3.15 \cdot \sin\phi_{13} + 3.29 \cdot \sin(\phi_{13} - \phi_{12}) \tag{3.19}$$

To be able to understand how the system behaves to the change of both phase shifts it is important to establish some operational points to be tested. In particular, the most interesting are the extreme operating cases, that is, when whether two ports transfer the maximum power among themselves without using the third port or when maximum general power transfer among all ports occurs, and in particular when two ports are equally feeding the third one at maximum power. Given these two guidelines, the following operating points can be established:

- Point O: No power transfer.
- Point A: Battery feeds the load at maximum power.
- Point B: PV panels and the battery equally feed the load at maximum power.
- Point C: PV panels feed the load at maximum power.
- Point D: PV panels feed both the load and the battery equally at maximum power.
- Point E: PV panels charge the battery at maximum power.

If the load is regenerative, two new operating points are to be taken into consideration:

- Point F: PV panels and the load equally charge the battery at maximum power.
- Point G: Load charges the battery at maximum power.

Using Equations 3.17, 3.18 and 3.19, the required phase shifts at each operating point can be computed. It is important to notice that, as the voltage port is fixed and the maximum power is established at 500 W, the currents at each operating point can be easily computed as to leave phase shifts the only unknown parameters. The values are presented in Table 3.1, which is included in the next subsection to ease the comparison process with the simulation values.

Figure 3.3 represents the theoretical values of the phase shifts at each operating point. The analysis of the data and its meaning will be done in more detail on the next chapter, as the designed converter is described there and, in this case, only a previous version is assessed corresponding to the reference article and further theoretical analysis would exceed the scope of the project.

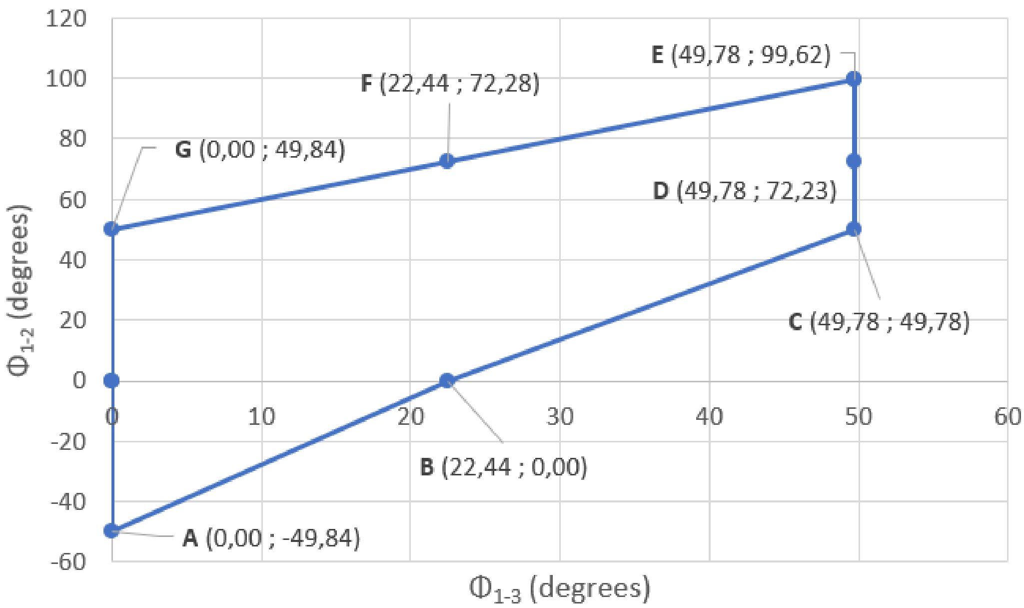

Figure 3.3: Phase shift values at different operating points for the 500 W converter.

3.2.2 Simulation and Comparison

After the theoretical analysis of the converter, the next step is to verify its functionality. Indeed, even though equations during theoretical computations have been reproduced form the reference paper, it is necessary to perform a simulation of the converter to verify if they are correctly stated. To do so, the LTSpice software is used to set up a simulation of the circuit, using the parameters of the reference paper.

The objective is to test the operating points that were defined in the previous section and compare the obtained values to the computations. Furthermore, a small comparison with the data given in the reference article [22] will be done to assess the similarities between the simulation and the reference article. No simulation was included in the reference paper, which arises the need for this test to be developed.

As waveforms will behave equally in both the reference design and the one that will be developed in the next sections, a detailed analysis will be done for the latter as its analysis is within the scope of the thesis. Therefore, the obtained currents and phase shifts for each operating point are shown in Table 3.2. Both power levels (in pu) and current values (in A) correspond to the input (respectively, output) of each port. A negative value of either power or current is related to that port functioning as a net consumer, that is, power is flowing to that port rather than from that port.

	P_1	P_2	P_3	I_1	I_2	I_3	ϕ_{13}	ϕ_{12}	ϕ_{23}
O	0,0	0,0	0,0	0,00	0,00	0,00	0,00	0,00	0,00
A	0,0	1,0	-1,0	0,00	13,89	-2,50	0,00	-49,84	49,84
B	0,5	0,5	-1,0	5,00	6,94	-2,50	22,44	0,00	22,44
C	1,0	0,0	-1,0	10,00	0,00	-2,50	49,78	49,78	0,00
D	1,0	-0,5	-0,5	10,00	-6,94	-1,25	49,78	72,22	-22,44
E	1,0	-1,0	0,0	10,00	-13,89	0,00	49,78	99,62	-49,84
F	0,5	-1,0	0,5	5,00	-13,89	1,25	22,44	72,28	-49,84
G	0,0	-1,0	1,0	0,00	-13,89	2,50	0,00	49,84	-49,84

Table 3.1: Power (pu), current (A) and phase shift (deg) operation for 500-W converter in theoretical computations.

	P_1	P_2	P_3	I_1	I_2	I_3	ϕ_{13}	ϕ_{12}	ϕ_{23}
O	0,0	0,0	0,0	0,00	0,00	0,00	0,00	0,00	0,00
A	0,0	1,0	-1,0	0,00	14,16	-2,50	1,26	-53,28	54,54
B	0,5	0,5	-1,0	5,03	7,04	-2,51	24,48	0,00	24,48
C	1,0	0,0	-1,0	10,07	0,00	-2,49	54,72	53,64	1,08
D	1,0	-0,5	-0,5	10,24	-6,99	-1,25	54,72	76,50	-21,78
E	1,0	-1,0	0,0	10,37	-13,87	0,00	54,72	105,48	-50,76
F	0,5	-1,0	0,5	5,32	-13,93	1,24	24,48	77,40	-52,92
G	0,0	-1,0	1,0	0,19	-13,90	2,51	0,00	54,72	-54,72

Table 3.2: Power (pu), current (A) and phase shift (deg) operation for 500-W converter in simulation.

Comparing the current values to the theoretical ones from Table 3.1, close similarities can be observed. A maximum of a 0.3 A difference is obtained for both ports 1 and 2, corresponding to the low voltage side (in point E, from 10 A to 10.37 A in port 1; in point A, from 13.89 A to 14.16 A in port 2). For port 3, the high voltage side, only a negligible difference of 0.01 A is observed when the port is injecting power into the system (point F and G).

As the maximum observed deviation only represents around a 3% difference, which can be assumed to be due to the choice of components in simulation (a simulation efficiency analysis will be performed in the coming sections), the values can be verified as equal in both the computations and the simulation.

To compare phase shift values, Figure 3.4 depicts the distribution of both phase shift 1-2 and 1-3 along the different operating points for both computations and simulation. The blue graph represent the theoretical values and is equal to Figure 3.3 shown in the previous subsection. The orange graph represents the newly obtained simulation values, numerically shown in Table 3.2. The distribution of the operating points, even though it is not clearly specified in the graph, is the same as in the previous section.

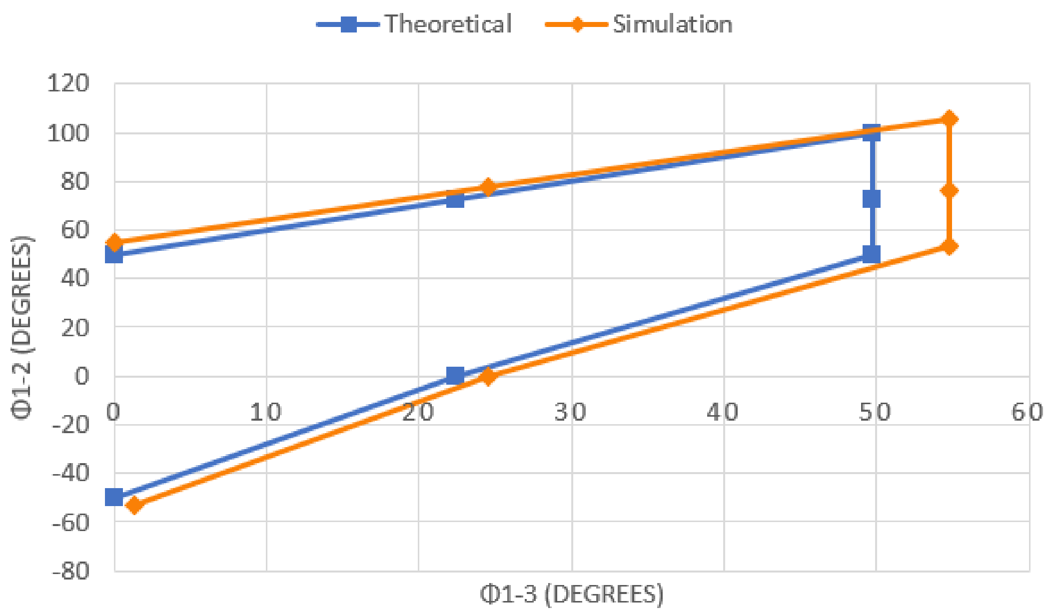

Figure 3.4: Phase shift comparison between theoretical computation and simulation.

Both graphs are shaped in a similar manner. Maximum difference is observed when phase shift 1-3 is maximum, which corresponds to operating points C, D and E. It is worth noting that these three points correspond to the maximum power on port 1 being transferred to either only port 2, port 3, or an equilibrium of the two. Nevertheless, as previously stated, no power transfer occurs directly from port 1 to port 2, and therefore all three operating points have a maximum power transfer from ports 1 to 3, and respectively, a maximum phase shift between the mentioned ports. It is assumable that port 1 has higher losses in simulation which induce these differences: this will be further explored in the efficiency analysis section.

It is important to assess that axis are not equally distributed: indeed, phase shift 1-2 has a higher difference in value when graph is moved the same distance in comparison to phase shift 1-3. This induces the misbelief that the beforementioned difference in phase shift 1-3 is drastically higher than the one in phase shift 1-2. When comparing them numerically, while the difference observed along the line C-D-E is of 4.94 degree for phase shift 1-3, the maximum difference in phase shift 1-2 is observed at operating point E and is of 5.86 degree, higher than the previous one. This point corresponds to the maximum value of the phase shift, as happened in the previous case. This graphical difference is due to the higher variability of phase shift 1-2, and it is therefore needed to have a tighter step in its axis.

All in all, it can be concluded that maximum difference between the theoretical values and the performed simulation occurs when the phase shifts are maximum. This occur simultaneously for both values in operating point E, where the difference is of almost 5 and 6 degree for phase shifts 1-3 and 1-2, respectively. Therefore this represents the critical point where simulation differs the most from analytical computations. This point is, as explained before, the maximum transfer from port 1 to port 2, which would physically mean the charge of the battery at maximum power exclusively from the solar panels.

Finally, a comparison with the specified obtained values in the reference article [22] is done. In particular, the article defines some values that were experimentally obtained, that is, measured on the built prototype. Not a lot of specific information is given, but nonetheless a comparison can be established to asses if the functionality of both is similar or if they differ at some level.

Regarding phase shift values, only two are specified. For operating point B, where ports 1 and 2 are equally sending power to port 3, the phase shift between the first two ports is zero degrees. Indeed, as can be seen in Table 3.2, at that point phase shift is null. This is to be expected: as power flowing both from port 1 and 2 to port 3 is the same, phase shift values are the same between these ports and the third one and, therefore, there is no phase shift between ports 1 and 2.

At operating point C, which represents port 1 feeding port 3 at maximum power without the use of port 2, again the phase shift between ports 1 and 2 is specified as 55 degree. In the simulation, as can be seen in the same Table 3.2, the obtained value is 53.64 degree. There is therefore a minimum difference, probably due to the experimental nature of the value in the reference paper. Phase shifts are expected to be a bit higher in practice as losses not taken into account in simulation are present and higher power will have to be transferred to obtain the desired level at the output. Furthermore, at that point, both the analyzed phase shift between ports 1-2 and the one between ports 1-3 is the same. As no power is present in port 2, its phase shift with port 3 must be null, which induces the equality mentioned before.

Besides these two phase shifts value, the peak normalized tank current for both ports is given. At each port, the value is found at the extreme operating point, which is when the analyzed port transfers maximum power to the third port (points C and A for ports 1 and 2, respectively). For port 1, the value given in the reference article is 17.8 A, while the obtained value during simulation is of 17.7 A. A perfect match can therefore be established.

In port 2, the given value in the paper is 25 A, while the one found during the simulation is 24 A. A small difference is observed which can be due to numerous factors, mainly the mentioned experimental nature of the paper data which implies higher losses and, consequently, higher power and current levels needed. As difference is not significant, a satisfactory comparison can be established as has happened with the other data analyzed. Simulation has been validated and the functionality of the converter, after the analysis performed in this section, can be assessed as expected.

As a final note regarding the tank currents, it is worth noting that their waveforms are a perfect sine, that is, no DC or offset value is present. The graphs shown in the reference article and the theoretical analysis point at the same form, which validates the obtained currents.

Chapter 4

Converter Design

4.1 Parameter Choice

The assessment of the topology using the same values as in the reference article was of key importance to understand its functionality and check the accuracy of the results exposed in the article. However, it is important to move forward from it and find the parameter choice that best suits the scope of this project. The maximum power level of the converter should be able to allow modularity, but at the same time not needing a too large amount of those modules for a simple application. Under this consideration, a 1 kW converter has been set as objective, which is double the power level of the reference article. As the power has been risen, the voltage level at all ports will be accordingly risen as to not create important differences in functionality when compared to the previous chapter.

Port 1 will be used to connect a PV system. Different systems and interactions can be established interconnecting PV cells and panels. The range available in the market extends to almost any capability, and high power levels can be achieved without having to increase systematically the rated voltage. Moreover, MPPT tracking allows for higher modularity in voltage and current levels while maximizing the power rating. After full deliberation of the actual capabilities and ranges available, a level of 60 V has been established for port 1.

Port 2 will be used to connect an energy storage system. As in the reference article, a battery set would represent the storage. Given that choice, and taking into account standard battery modules of 12 V, a level of 48 V will be assessed. As the general power has risen, the previous 36 V has to be improved. The choice of 48 V is motivated by the inclusion of an extra module compared to the reference article. Another module would rise the voltage to the same level as in port 1, which would reduce its interest as both ports would have the same parameters.

Port 3 will be used for the DC distribution of the building. This distribution is typically established at 400 V for DC, and therefore that level will be chosen. The interest of this third port for our design is beyond the load capability, as the bidirectionality of the port is intended to be able to interconnect different converters and exchange power among themselves. It will be therefore designated as distribution port rather than load port from now on, and it would also be a way to differentiate the reference article design and the projected one.

4.2 Theoretical Analysis

To compute the different parameters, the same procedure as in the previous section will be used. The only changes to be introduced during computation are the new port voltages and the maximum load power. Firstly, the transformer turns ratios are computed:

$$n_{13} = \frac{V_1}{V_3} = \frac{60\ V}{400\ V} = 0.15 \tag{4.1}$$

$$n_{23} = \frac{V_2}{V_3} = \frac{48\ V}{400\ V} = 0.12 \tag{4.2}$$

The equivalent inductance corresponding to the maximum load is then found:

$$Z_o = \frac{V_3^2}{P_3} = \frac{(400\ V)^2}{1000\ W} = 160\ \Omega \tag{4.3}$$

Maintaining the same conditions as in the previous case, those are, having quality factors at maximum load at 4.0 and a ratio of switching to resonant frequency of 1.1, the resonant tank parameters are set:

$$\begin{cases} \dfrac{1}{\sqrt{L_i \cdot C_i}} = \dfrac{2 \cdot \pi \cdot 100\ kHz}{1.1} = 571198\ \dfrac{rad}{s} \\ \dfrac{\sqrt{\dfrac{L_i}{C_i}}}{\left(\dfrac{8}{\pi^2}\right) \cdot 160\ \Omega \cdot n_{i3}^2} = 4 \end{cases} \tag{4.4}$$

Given that the turns ratios are established as $n_{13} = 0.15$ and $n_{23} = 0.12$ as previously stated, the resonant tank parameters are the following:

$$\begin{matrix} L_1 = 20.43\ \mu H & L_2 = 13.08\ \mu H \\ C_1 = 0.15\ \mu F & C_2 = 0.23\ \mu F \end{matrix} \tag{4.5}$$

The impedances of each resonant tank can be directly computed:

$$\begin{aligned} Z_1 &= \sqrt{\frac{L_1}{C_1}} = \sqrt{\frac{20.43\ \mu H}{0.15\ \mu F}} = 11.67\ \Omega \\ Z_2 &= \sqrt{\frac{L_2}{C_2}} = \sqrt{\frac{13.08\ \mu H}{0.23\ \mu F}} = 7.54\ \Omega \end{aligned} \tag{4.6}$$

The currents at all ports can be computed following the detailed procedure of the previous section:

$$\begin{aligned} I_1 &= \frac{8}{\pi^2} \cdot \frac{n_{13} \cdot V_o}{Z_1 \cdot (F_1 - ({}^1/_{F_1}))} \cdot \sin \phi_{13} = \\ &= \frac{8}{\pi^2} \cdot \frac{0.15 \cdot 400}{11.67 \cdot (1.1 - ({}^1/_{1.1}))} \cdot \sin \phi_{13} = 21.83 \cdot \sin \phi_{13} \end{aligned} \tag{4.7}$$

$$\begin{aligned} I_2 &= \frac{8}{\pi^2} \cdot \frac{n_{23} \cdot V_o}{Z_2 \cdot (F_2 - ({}^1/_{F_2}))} \cdot \sin (\phi_{13} - \phi_{12}) = \\ &= \frac{8}{\pi^2} \cdot \frac{0.12 \cdot 400}{7.54 \cdot (1.1 - ({}^1/_{1.1}))} \cdot \sin (\phi_{13} - \phi_{12}) = 27.03 \cdot \sin (\phi_{13} - \phi_{12}) \end{aligned} \tag{4.8}$$

$$I_3 = n_{13} \cdot I_1 + n_{23} \cdot I_2 = 0.15 \cdot I_1 + 0.12 \cdot I_2 = 3.275 \cdot \sin \phi_{13} + 3.244 \cdot \sin (\phi_{13} - \phi_{12}) \tag{4.9}$$

Using Equations 4.7, 4.8 and 4.9, the required phase shifts at each operating point can be computed as in the previous section. Each operating point was also previously explained. The values are presented in Table 4.1. Figure 4.1 represents the theoretical values of the phase shifts at each operating point. The perimeter of the graph delimits the operating region of the converter.

	P_1	P_2	P_3	I_1	I_2	I_3	ϕ_{13}	ϕ_{12}	ϕ_{23}
O	0,0	0,0	0,0	0,00	0,00	0,00	0,00	0,00	0,00
A	0,0	1,0	-1,0	0,00	20,83	-2,50	0,00	-50,41	50,41
B	0,5	0,5	-1,0	8,33	10,42	-2,50	22,43	-0,24	22,67
C	1,0	0,0	-1,0	16,67	0,00	-2,50	49,79	49,79	0,00
D	1,0	-0,5	-0,5	16,67	-10,42	-1,25	49,79	72,46	-22,67
E	1,0	-1,0	0,0	16,67	-20,83	0,00	49,79	100,20	-50,41
F	0,5	-1,0	0,5	8,33	-20,83	1,25	22,43	72,84	-50,41
G	0,0	-1,0	1,0	0,00	-20,83	2,50	0,00	50,41	-50,41

Table 4.1: Power (pu), current (A) and phase shift (deg) operation for 1-kW converter.

Some conclusions on the functionality of the converter can be extracted from these data. The power given by port 1 is directly related to the phase shift between ports 1 and 3. Indeed, a 22.43 degree implies that the port is generating half the maximum power, while the maximum power is given at 49.79 degree. Similarly, port 2 depends directly on the phase shift between ports 2 and 3. In this case, a 22.67 degree shift implies that the port is giving half the maximum power, while the maximum is achieved at 50.41 degree. If the port is consuming power rather than generating, the absolute values of the phase shift are the same but changing its sign.

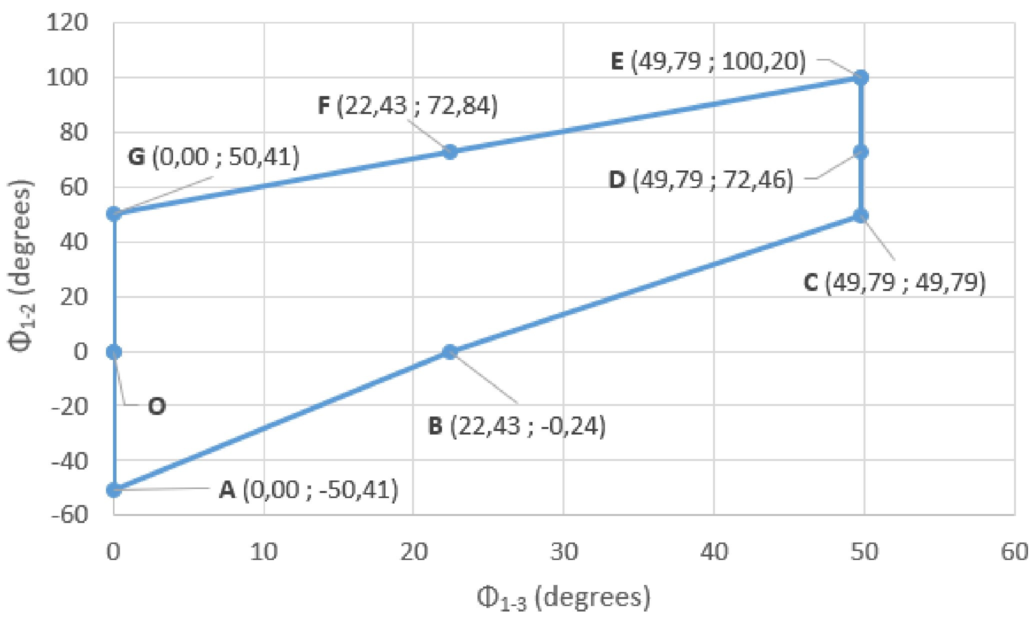

Figure 4.1: Phase shift values at different operating points for the 1 kW converter.

Besides this direct correlation in magnitude, it can also be concluded that the port consuming power has to lag the port which is providing the power, when comparing the control signals of the active bridges. If there is no phase shift among two ports, no power transfer occurs, whereas when one bridge starts lagging another, a power transfer is created.

A second conclusion is that no power transfer is done between ports 1 and 2: indeed, when power is transferred between these two ports, it has to go through port 3. This can be easily seen, for example, in operating point E: even though port 3 has no power, both phase shift 1-3 and 2-3 are at maximum value, as port 1 is feeding port 2 at maximum power and, therefore, the power flow has to go through port 3. Phase shift between ports 1 and 2 is therefore not meaningful and it just represents the difference between the other two phase shifts. However, as port 1 is taken as the reference signal, all computations are referred to phase shifts 1-2 and 1-3. This is the main reason of having these two phase shifts represented in Figure 4.1.

It is also interesting to compare both low voltage side ports. Their phase shift values are really similar in magnitude, with just a small deviation lower than one degree. Their functionality is therefore basically the same. Port 3 however does not behave in the same manner. As equilibrium has to be respected at all times (that is, injected power has to equal the consumed power), it is not possible to directly control the three ports individually. It is possible, however, to modify the two meaningful phase shifts (1-3 for port 1 and 2-3 for port 2) to control the third port at will throughout all the operating region. An example could be operating point F: as port 2 is consuming maximum power, its phase shift (2-3) is maximum and negative, whereas port 1 is injecting half the maximum power, and therefore its phase shift (1-3) is at half its top value. The rest of the power will have to be fed by port 3, which implies that we are indirectly establishing port 3 at a level of half the maximum power.

4.3 Simulation Design

After the design and theoretical computation of the converter, a simulation of its functionality is to be analyzed, as it was done for the reference design. To produce the simulation, the LTSpice software is once again used, which allows to view the voltage and current signals at any point of the converter circuit, among other features. First, a small description of the elements used during the simulation and the reasoning behind their choice is done.

All ports inputs (respectively, outputs) are represented as either voltage sources, if they are generating power, or resistances, if they are consuming power. A filter capacitor is put in both ports 2 and 3 as they can function as outputs and, therefore, they require it to rectify the signals and get a DC voltage at the port. No filter is required in port 1 as it is intended to connect the PV panels and, therefore, no bidirectionality is expected. Filtering capacitor parameters can be twisted to obtain the desired maximum voltage ripple. In particular, at the low voltage side, ripple will be maintained below 0.5 V, while in the high voltage side, it will be set at a maximum of 1 V.

The full-bridges are made of four MOSFETs and diodes each. To select the components in simulation, the same have been chosen for both low voltage ports (1 and 2) and different ones for the high voltage port (3) to allow it to work properly. Components already included by default in the software have been chosen to ease selection. A range of products from different manufacturers is already available, from which the selection is to be made according to its parameters.

In the low voltage side, the chosen MOSFET reference is BSC196N10NS, manufactured by Infineon. It has a V_{ds} voltage of 100V, high enough for both ports, and a low R_{dson} of 20 mΩ. The chosen diode reference is MBR20100CT, type Schottky and of On-Semi manufacturer. It has a breakdown voltage of 100V which is again high enough for both ports.

In the high voltage side, the chosen MOSFET reference is STP8NM60, manufactured by ST. The V_{ds} voltage level is 650 V, high enough for the 400 V nominal voltage of the port. Its R_{dson} is of 0.9 Ω, one of the lowest available for the rated voltage in the software. The diodes are of reference RFU20TM5S, by Rohm manufacturer, of the FastRecovery type. Its breakdown voltage is 530 V which ensures normal operation under nominal voltage with a large margin.

To control each MOSFET, a voltage source is used, connected between the gate and the source to activate the device at will. The voltage level depends on the threshold of each device, and it has to be chosen high enough to reach the mentioned level. It has been established at 12 V for the low voltage side and 10 V for the high voltage side, after carefully assessing their datasheet specifications. The sources are defined to produce square signals at fixed 0.5 duty cycle as required for the converter. A small deadtime of 20 ns is introduced to ensure that the high side and low side MOSFETs do not conduct at the same time, as a shortcircuit would be created.

A time delay on each voltage source is introduced to control the desired phase shift. Within each port, each half bridge is delayed half a period between themselves to have the desired output. Between ports, a delay is introduced to assess the desired phase shift. As the period is fixed at 10 μs, a delay of 2.5 μs would be equivalent to a phase shift of 90 degree, as an example. Port 1 delay is not changed as it is the reference port. To change the phase shifts easily, LTSpice formulae option can be used to modify all control sources within the same bridge together.

Both resonant tanks are simply simulated as a capacitor and inductor with the computed values of previous sections. The three-winding transformer is simulated in the software as three magnetically coupled inductors with inductance values equal to the square of the desired ratio. The simulation time is left running long enough to achieve steady state operation, which is generally around 5-10 ms, depending on the operation point. After that time, the converter has achieved stability and the analysis can be performed accordingly.

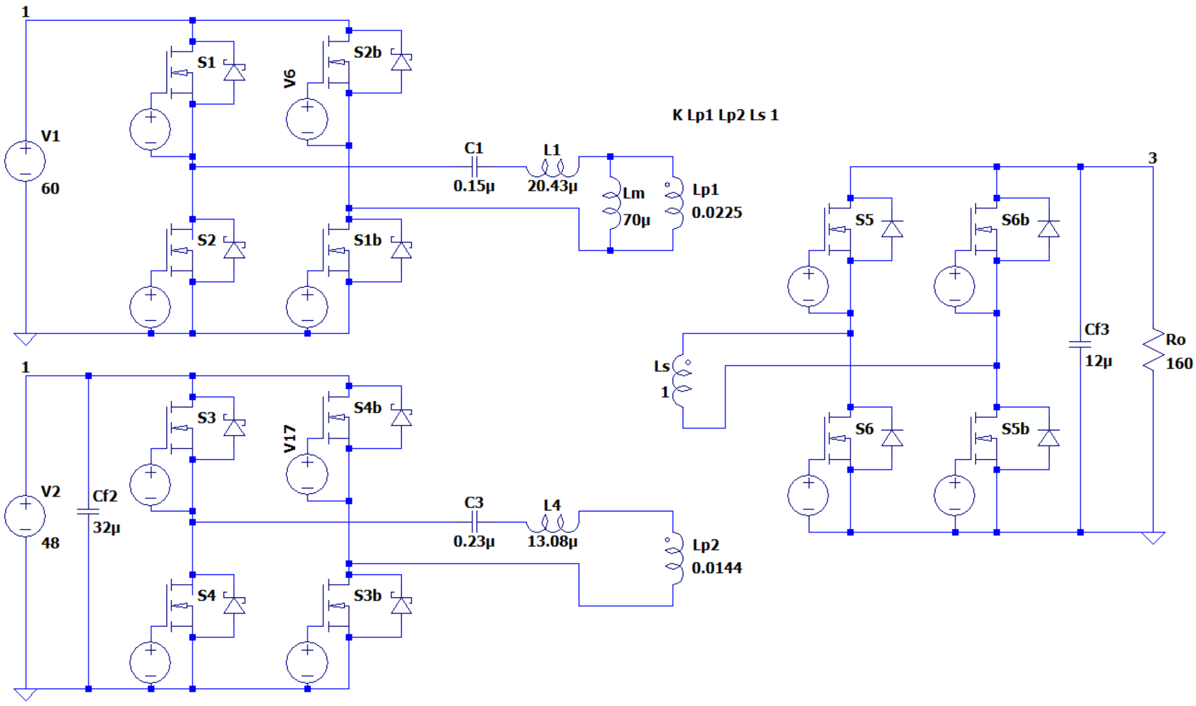

Figure 4.2: Converter circuit as designed in LTSpice for simulation.

4.4 Waveforms Analysis

The LTSpice software allows to get the values and waveforms of voltages and current at all points of the circuit while changing the parameters at will. To do a structured analysis, different sections will be differentiated. In this section, a waveform analysis of three operating points will be performed. The choice of analyzing three points instead of all the previously defined ones is due to the manageability of the data. Too many selected points would result in a long and repetitive analysis that may be counterproductive if the intention is to understand the functionality of the converter. The selected operating points are intended to be also the ones that will be validated experimentally during the testing phase of the prototype.

The choice of the operating points to be tested has been done under two main criteria. On the one hand, it is important to test all bidirectional ports (battery and distribution ports) in both operating conditions. On the other hand, extreme cases are to be tested to see how the converter behaves under such circumstances. Extreme cases are referred to when either one port is fully feeding another port without the use of the third one, or two ports are equally feeding the third, resulting in a maximum power transfer throughout the converter. These criteria were also followed when selecting all the operating points as was mentioned in previous sections.

The first selected operating point is B, which represents ports 1 and 2 equally feeding the third port at maximum power (practically, it would represent both PV panels and the battery feeding the DC distribution line). Next, operating point E is selected, in which port 1 is fully feeding port 2 at maximum power without using the third port (it would represent the PV panels charging the battery). Finally, operating point G has been selected, in which port 3 is fully feeding port 2 (the distribution line charging the battery).

Each analyzed operating point will include five graphs. The first two correspond to the voltage and current levels at the transformer windings of each port. Three signals will be displayed: a blue signal corresponding to port 1, red signal corresponding to port 2 and green signal corresponding to port 3. The three latter graphs include the same information but displayed separately for each port. In those, the blue signal corresponds to the voltage level and the red signal to the current wave. The legend at each graph will display it in an orderly manner. All graphs have also been taken between the 9.96 ms and 10 ms points to ensure that steady state has been reached, including therefore four periods of each wave.

4.4.1 Operating Point B

In operating point B, ports 1 and 2 equally share the maximum load on port 3, that is, ports 1 and 2 feed port 3 at half the maximum power each. Practically, it would represent having the PV panels and the battery feeding the distribution line. This condition allows to see how differently both ports behave to produce the same amount of power. A slight change in phase shifts would turn the dominance to either one of the ports and break the tested equilibrium.

The phase shift corresponding to the described operating point is 23,40° for port 3 and 1,80° for port 2, both referencing to port 1 as in previous cases. The values are similar to the theoretical ones: ports 1 and 2 have a small 'offset phase shift' to reach equilibirum of their power levels while port 3 has an almost equal shift on both ports 1 and 2, as was to be expected.

Figure 4.3 represents the voltage levels of each port at the transformer winding side, that is, after the effect of the full-bridge for ports 1 and 2 and before its effect on the consuming port 3. All voltages have the desired levels of 60 V, 48 V and 400 V respectively for each port, with perfectly symmetrical square signals that are shifted as was previously described. The period of all signals is 10 μs, according to the 100 kHz switching frequency.

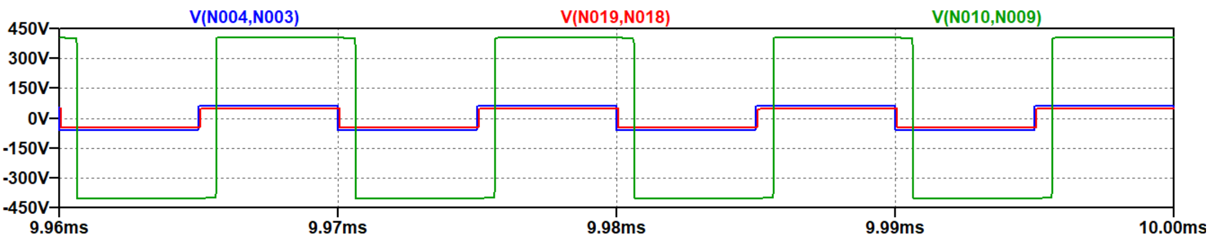

Figure 4.3: Voltage levels per port at the transformer at operating point B.

Figure 4.4 represents the current signals at the transformer windings. In the case of the first two ports, it also represents the current flowing through the resonant tanks. All signals are perfect sine waves. Ports 1 and 2 are opposing port 3 wave, that is, they are always sign inverted, as the first two ports are feeding power and the third one is consuming it. The current levels are 8.99 A at port 1 and 11.64 A at port 2 which, after transforming through the corresponding turns ratio, account each approximately for half the 2.5 A current level of port 3.

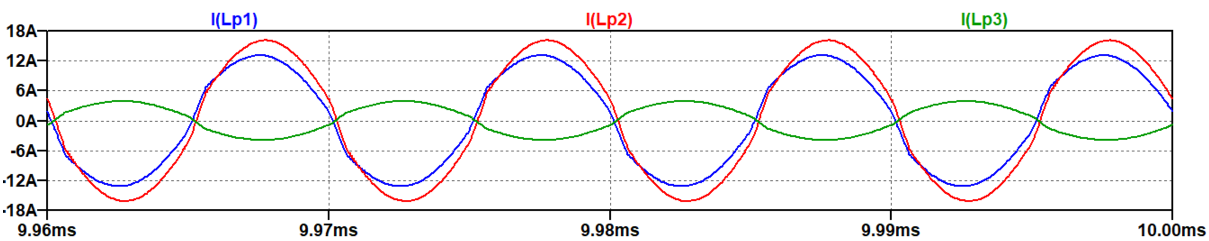

Figure 4.4: Current levels on each tank and transformer side at operating point B.

Figure 4.5 represents the voltage and current level of port 1 at the transformer winding. This graph allows to verify how the current is lagging voltage at the port. As was stated in previous sections, this condition is unavoidable to be working under ZVS conditions.

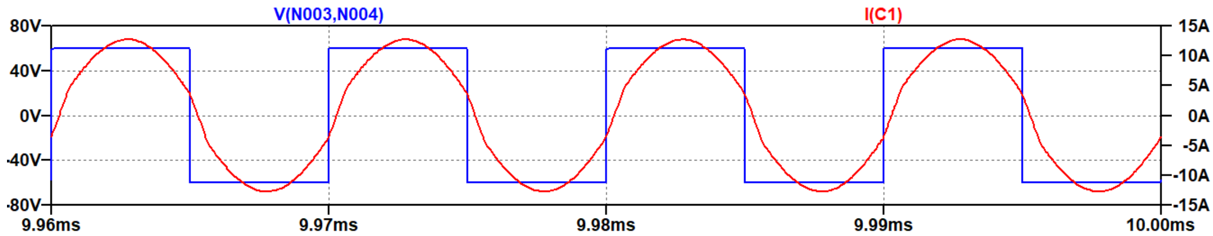

Figure 4.5: Voltage and current level at transformer for port 1 at operating point B.

Figure 4.6 represents the voltage and current levels at the transformer winding of port 2. As was the case for the previous port, current is lagging voltage and, therefore, it is working under ZVS condition.

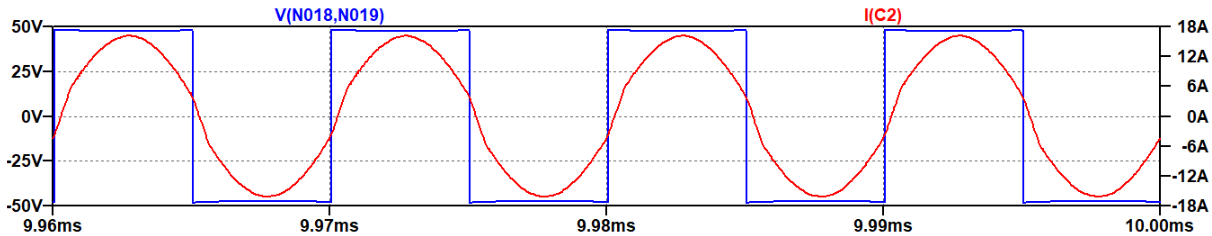

Figure 4.6: Voltage and current level at transformer for port 2 at operating point B.

Figure 4.7 represents the voltage and current levels at the transformer winding of port 3. In this port, as was stated during theoretical analysis, voltage must lag current to be under ZVS. This is due to the definition of the current that was made: the current is taken as leaving the transformer winding instead of going into it as happened for the previous ports. Therefore, ZVS condition is also met in this port, and all the converter is working under lossless switching.

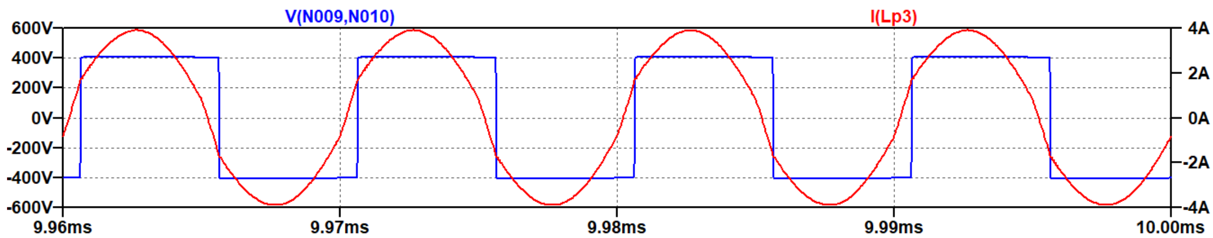

Figure 4.7: Voltage and current level at transformer for port 3 at operating point B.

4.4.2 Operating Point E

In operating point E, port 1 is feeding port 2 at maximum power without any contribution from port 3. Practically, this would represent the PV panels charging the battery at full power without the distribution side. As has been previously stated, and will be seen in this section, even though no power contribution is made by port 3, power does flow through the port as no transfer is done directly from port 1 to port 2.

Phase shift corresponding to this operating point is 53.28° for ports 1-3 and 97.56° for ports 1-2. Values are similar to the theoretical ones and yield the same interpretation. Phase shift between ports 1-3 is the maximum phase shift found in all points as it is transferring its maximum power. Phase shift 1-2 can be interpreted as the sum of phase shifts 1-3 and 3-2, as power has to flow through port 3 to reach port 2. Therefore, phase shift between 3-2 is also maximum and translates into a maximum phase shift 1-2. In later sections, phase shift values will be further discussed and compared among all operating points.

Figure 4.8 represents the the voltage levels of each port at the transformer windings. Each port has a perfect symmetrical square signal fixed at the desired voltage level (60 V, 48 V and 400 V respectively) and phase-shifted accordingly as described before.

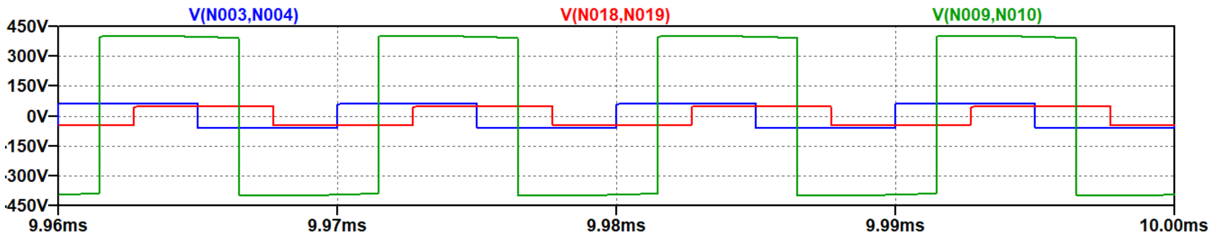

Figure 4.8: Voltage levels per port at the transformer at operating point E.

Figure 4.9 represents the current levels of each port at the transformer windings. For the first two ports, it also represents the current through the resonant tank, as it is in series with the transformer winding. Current level of port 1 is 20.33 A, on port 2 it is 20.83 A opposing port 1 current, and the level at port 3 is 0 A.

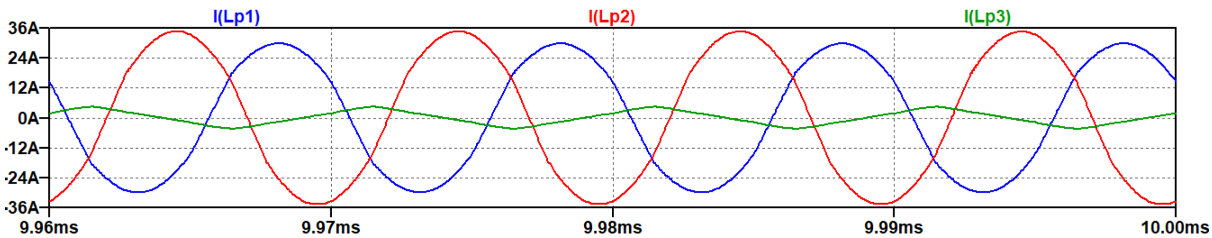

Figure 4.9: Current levels on each tank and transformer side at operating point E.

Figure 4.10 represents the voltage and current levels of port 1 at the transformer winding. As was reviewed during the analysis of the previous operating point, in order to assess that ZVS is occurring, current must be lagging its respective voltage. As can be observed, it is indeed the case and therefore port 1 is operating under ZVS conditions.

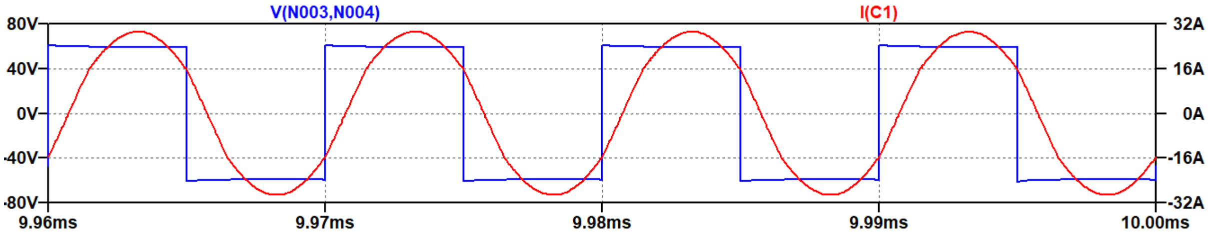

Figure 4.10: Voltage and current level at transformer for port 1 at operating point E.

Figure 4.11 represents the voltage and current levels of port 2 at the transformer winding. Similarly to the previous port, the current signal is lagging its voltage and, therefore, the port is also operating under ZVS condition.

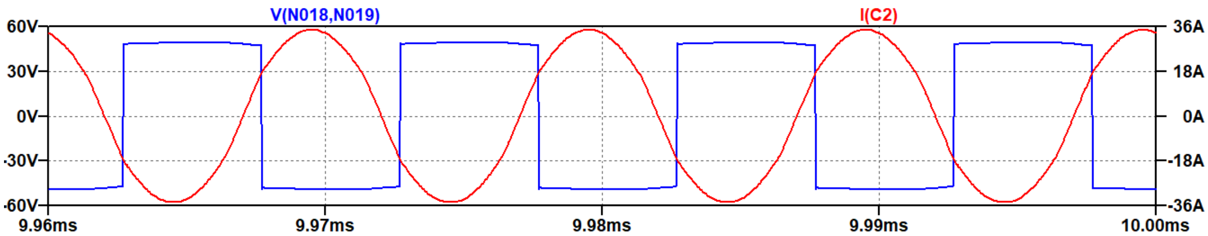

Figure 4.11: Voltage and current level at transformer for port 2 at operating point E.

Figure 4.12 represents the voltage and current levels of port 3 at the transformer winding. The current in this case is of triangular shape rather than sinusoidal. It could be due to the fact that the other two ports have their currents opposing each other, at an almost perfect 180 degree shift, which could lead to this triangular behaviour at the third winding of the transformer. As was explained in the previous operating point, and related to the definition of the port 3 current which is opposed to ports 1 and 2, voltage must be lagging the current to assess that ZVS is indeed occurring. As it is the case, port 3 is operating in lossless conditions and therefore all converter is working under that circumstance as was expected.

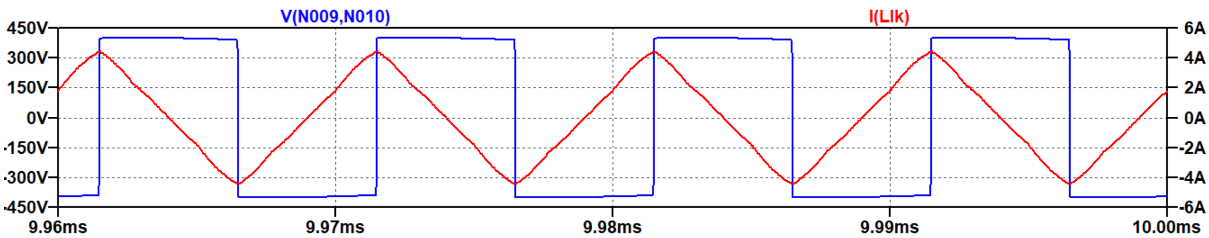

Figure 4.12: Voltage and current level at transformer for port 3 at operating point E.

4.4.3 Operating Point G

In operating point G, port 3 is feeding port 2 at maximum power without the intervention of port 1. Practically, this would imply that the distribution side is injecting power at maximum level to feed the battery without the involvement of the PV panels. It is both a similar and an opposing case to the last analyzed point: battery is being charged at full power on both cases but the power source has changed from one port to the other.

Phase shifts are 0° for ports 1-3 and 47.52° for ports 1-2. As no power transfer is done between ports 1-3, no phase shift is needed. On ports 1-2, phase shift does not represent a direct power transfer between them as has been stated in previous occasion. Instead, it only represents the phase shift between ports 2-3 (as 1-2 is null), which is maximum as the power transfer. Its value is close to the theoretical one and therefore behaves as expected.

Figure 4.13 represents the voltage levels of each port at the transformer windings. These are once again perfect symmetrical square signals at the fixed levels for each port (60 V, 48 V and 400 V, respectively). Each signal has a delay corresponding to the fixed phase shift. In particular, third port signal has no delay when compared to the reference signal, which is port 1, and port 2 signal has a delay of 1.32 μs, which correspond to the mentioned phase shift.

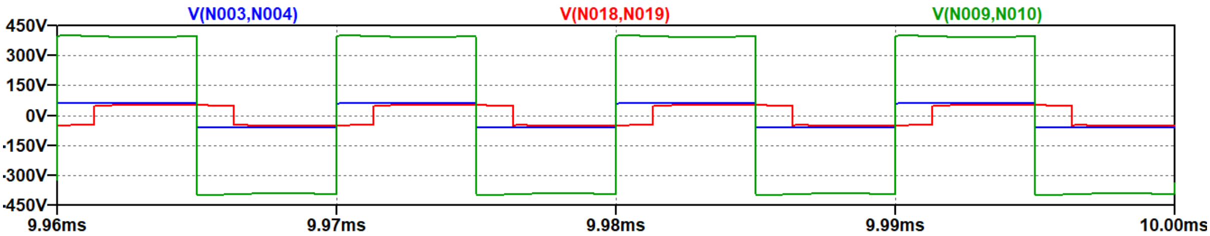

Figure 4.13: Voltage levels per port at the transformer at operating point G.

Figure 4.14 represents the current levels of each port at the transformer winding. For the first two ports, this also equals the current levels at the resonant tanks. While port 1 current is almost null (there is a small offset of 0.12 A value that accounts for its own losses), ports 2 and 3 are opposing as happened in other operating points when ports where net producers and consumers of power. The levels are 20.81 A and 2.55 A, respectively.

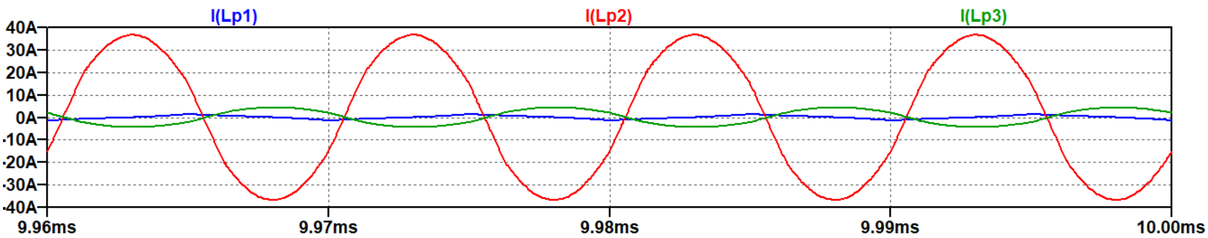

Figure 4.14: Current levels on each tank and transformer side at operating point G.

Figure 4.15 represents the voltage and current levels of port 1 at the transformer winding. Even though current level on port 1 is almost null as it does not produce nor consume power, the small power generated and consumed within the bridge of the port presents a current that is lagging the voltage. Therefore, ZVS conditions are also met in port 1.

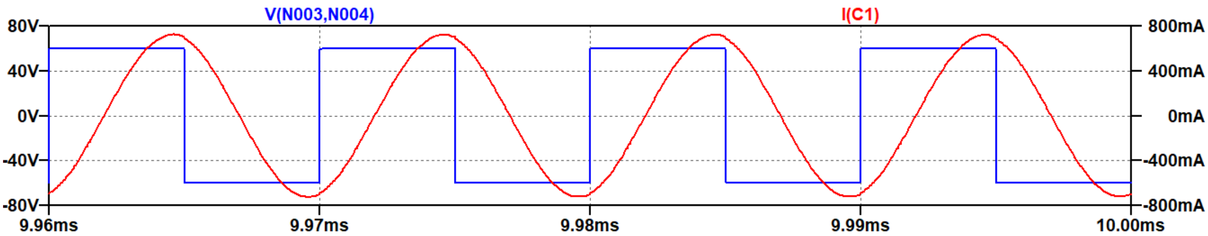

Figure 4.15: Voltage and current level at transformer for port 1 at operating point G.

Figure 4.16 represents the voltage and current levels of port 2 at the transformer winding. As was the case in the previous port, current is once again lagging its respective voltage and ZVS is occuring on port 2.

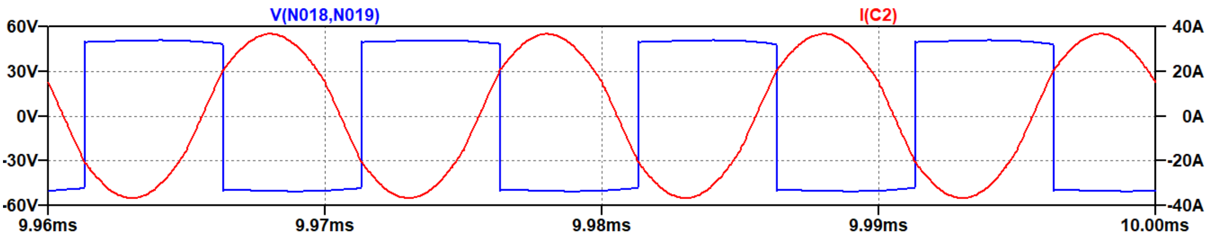

Figure 4.16: Voltage and current level at transformer for port 2 at operating point G.

Figure 4.17 represents the voltage and current levels of port 3 at the transformer winding. As voltage is lagging the current, which is the condition under the definition of the port 3 current for ZVS, the lossless switching operation is verified for all ports of the converters. It has also been verified for all three analyzed operating points, which implies that ZVS is ensured during all operating region under the designed constraints of the converter.

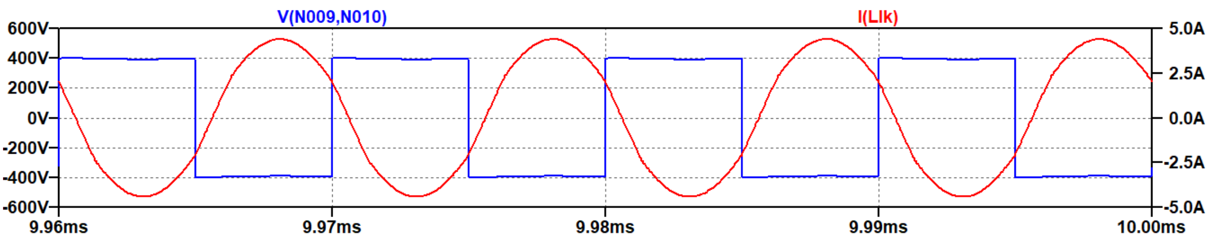

Figure 4.17: Voltage and current level at transformer for port 3 at operating point G.

4.5 Result Comparison

In the next section, an analysis of the operating points will be performed, with a summary table of the obtained currents and phase shifts and a graph comparing the phase shift values with the theoretical computations. Furthermore, a comparison with the previously described theoretical results is of interest to assess if the simulation indeed yields the same conclusions.

Table 4.2 represents the power (in pu), current (in A) and phase shift (in degree) corresponding to each operating point analyzed. The point nomenclature corresponds to the order described during theoretical computations. It can be nonetheless understood from the power values of each port: 1 pu symbolizes the maximum power, while 0.5 is half of it and 0 is, of course, no power. A negative value indicates that the corresponding port is consuming power, while positive values are the injections unto the converter.

	P_1	P_2	P_3	I_1	I_2	I_3	ϕ_{13}	ϕ_{12}	ϕ_{23}
O	0,0	0,0	0,0	0,00	0,00	0,00	0,00	0,00	0,00
A	0,0	1,0	-1,0	0,57	25,46	-2,50	0,61	-46,80	47,41
B	0,5	0,5	-1,0	8,99	11,64	-2,50	23,40	1,80	21,60
C	1,0	0,0	-1,0	19,80	0,00	-2,50	53,28	52,63	0,65
D	1,0	-0,5	-0,5	20,01	-10,53	-1,25	53,28	73,26	-19,98
E	1,0	-1,0	0,0	20,33	-20,83	0,00	53,28	97,56	-44,28
F	0,5	-1,0	0,5	8,46	-20,90	1,30	23,40	70,20	-46,80
G	0,0	-1,0	1,0	0,12	-20,81	2,55	0,00	47,52	-47,52

Table 4.2: Power (pu), current (A) and phase shift (deg) operation for 1-kW converter in simulation.

An initial analysis of the phase shifts can be done to understand how the converter behaves. Power transfers occurs between ports 1-3 and 2-3, with no direct power transfer between ports 1-2. That feature can be seen in the direct correlation of power transfers and the two mentioned phase shifts. However, the phase shifts controlled are always 1-2 and 1-3, as port 1 is taken as reference for ease of computations.

Regarding port 1, its power transfer is directly related to phase shift 1-3: when there is no power transfer, no phase shift occurs, while when the port is feeding half or full maximum power, phase shift is 23.40° or 53.28°, respectively. The port that is consuming the power does not affect at all the value of the phase shift. This port does not have bidirectional operation as it is practically representing PV panels and there is no interest in feeding power to the panels.

Port 2 has its power transfer directly related to phase shift 2-3. Indeed, no power transfer is indicated by a null phase shift, while half and full maximum power are 21.60° and 47.41° respectively. It is interesting to notice that in this case small differences are observed among the same power transfer depending on the emitting/recieving ports. One simple explanation would be related to the bidirectionality nature of this port when compared to port 1, which makes the phase shifted vary between 2-3 degree among operating points of the same power transfer.

Port 3 power is defined by the other two power transfers. As equilibrium has to be always respected (injected and consumed powers must equal zero), its power is directly related to the other two ports. If, for example, port 1 wants to feed the other two ports at maximum power, phase shift 2-3 must be regulated to decrease the power transfer to port 2 which, maintaining the other phase shift, would imply an increase on the power transfer to port 3. All operating points and power transfers can therefore be controlled with just two phase shifts.

Figure 4.18 represents a comparison between the theoretical phase shifts found in the previous chapter to the simulated results that were just analyzed. The represented phase shifts are the corresponding to ports 1-2 and 1-3, as they are the ones that are directly changed during both computation and simulation.

Small differences can be observed throughout all the operating region. While phase shift 1-3 is slightly higher in simulation at all points, phase shift 1-2 experiences the contrary effect and has a slightly lower value in simulation at almost all operating points. While difference in the first phase shift is due to the inclusion of losses within the simulation that are not taken into account in theoretical computations (maximum difference is about 3 degree, which corresponds at when maximum power is transferred and, therefore, maximum losses occur), second phase shift deviations are of different nature.

Phase shift 1-2 is not directly related to any power transfer, but it is rather a sum of the other two. As a consequence, its variability is slightly higher and can go both higher or lower than the theoretical value. However, a direct correlation to overall power transfer is still observed: the maximum difference, of 3°, occurs in operating point E, when both ports 1 and 2 are transferring the maximum rated power. It is therefore consequent with the nature of the converter and the conclusions extracted and mentioned before.

Overall, differences are not considerably high, which indicates that both theoretical analysis and simulation concur within the same converter. This feature validates the performed simulation and is a strong indicator that both the design and the simulation have been well made.

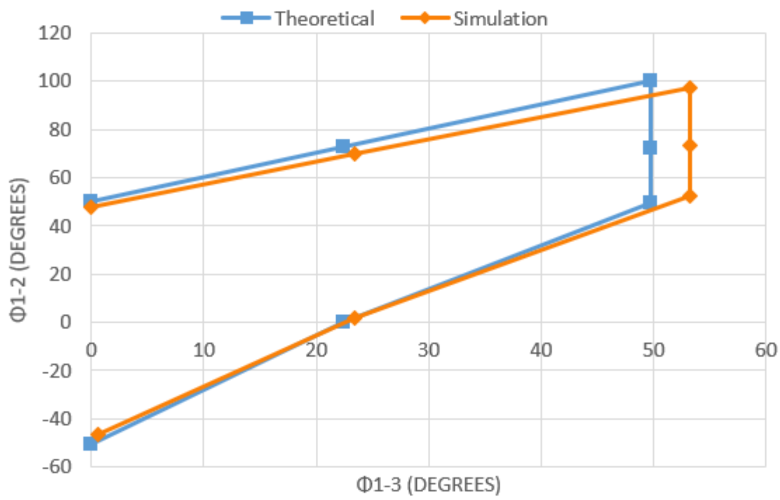

Figure 4.18: Phase shift comparison between theoretical computation and simulation.

4.6 Voltage Range

The functionality of the converter has been tested and validated in the previous subsection. The focus is now turned unto how the converter works under circumstances that are not the nominal ones for which it has been designed. Firstly, a voltage range test is performed to asses how much the voltage may change from the rated one while still being able to work throughout all the operating region.

The main idea is to test the different ports at their most demanding operating point and reduce the voltage level until, even with the maximum power transfer, it is not able to inject the required power. Maximum power transfer occurs, as was previously stated, when the respective phase shift is 90º.

Port 1 has been tested under operating point C, where it is injecting the maximum power to be consumed by port 3. Under these circumstances, phase shift 1-3 has been set at 90 degree for maximum power transfer and the voltage level of port 1 has been reduced until the 1kW power level is achieved. The minimum voltage has been found at 49 V, which represents a 35 A current through its resonant tank.

Under these circumstances, it is important to assess if the converter is still working under lossless conditions, that is, under ZVS. As was the case in the previous subsection, ZVS occurs in ports 1 and 2 when current lags its applied voltage, and in port 3 when the opposite occurs. While for both ports 1 and 3 the ZVS conditions are still met, it is not the case for port 2, as can be seen in Figure 4.19.

As current is not lagging its applied voltage, there is a discontinuity in its sine wave, which creates some switching losses. The spike on the current is due to the fact that the conducting diode is releasing its stored energy, as hard switching occurs. As it occurs in the port that is not transferring power, the current value is close to zero. Furthermore, it is a sign that the converter has been well designed, as moving outside the established voltage does indeed not guarantee a lossless operation.

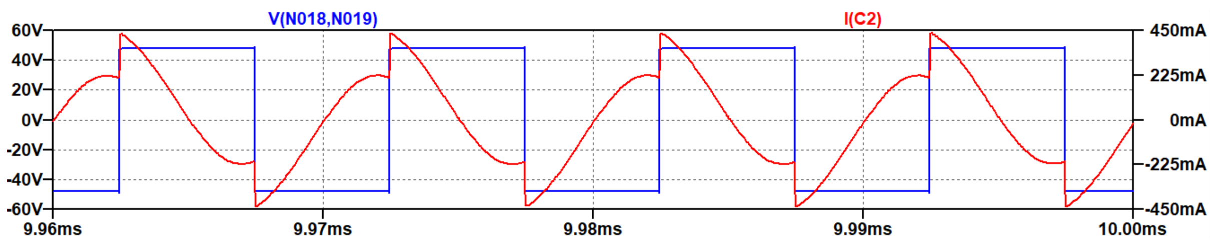

Figure 4.19: Voltage and current level at transformer for port 2 when $V_1 = 49V$.

Port 2 has been tested under operating point A, which represents the battery feeding the distribution side at maximum power and no contribution from the PV panels. Practically, ports 2 and 3 are at maximum power transfer while port 1 does not intervene. As happened in the previous test, this operating point represents the most demanding situation for port 2, and is therefore suitable to test how much the voltage level of the port can decrease while maintaining the desired power transfer.

The lower voltage limit has been found at 36.5 V, which represents the voltage level at which a 90 degree phase shift between ports 2 and 3 induces a power transfer equal to the maximum rated power, that is, 1 kW. The current level is 40 A through the resonant tank. As has been previously done, it is important to assess how the currents and voltages at each port are affected by this excepcional operation and, in particular, if ZVS conditions are still met.

While the two active ports are working at lossless switching, port 1 does not. In this port, as can be seen in Figure 4.20, current is not lagging voltage but rather the opposite is happening. A discontinuity in the current sine wave occurs when the square voltage transients from its negative value to its positive, creating some losses at that switching point. These losses occur at the port that is not involved in the power transfer and, therefore, current is almost null and the losses are negligible. Converter can also work fine under these special circumstances without further problems.

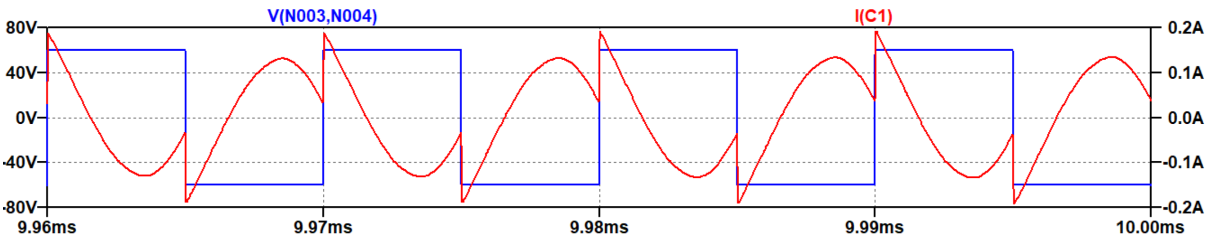

Figure 4.20: Voltage and current level at transformer for port 1 when $V_2 = 36.5V$.

Port 3 has been tested under operating point G, that is, when the distribution line is charging the battery at full power. This would imply that port 3 is transferring the maximum power to port 2 without the intervention of port 1. Once again the idea is to lower the voltage level until the maximum phase shift corresponds to the maximum power in order to find what is the lowest voltage possible that maintains operation.

The lower limit has been established at 300 V, representing a 4.5 A current at the transformer winding. After checking ZVS operation at all ports, it has been assessed that the converter is still working under lossless conditions. This difference with the other two checked limits, in which ZVS was lost, can be due to the fact that the resonant tanks are present in ports 1 and 2, which are in this case both at their rated voltage level. Even though port 3 voltage is changed, there is no resonant tank in the port which could relate to a more flexible operation regarding the voltage level.

Some final conclusions and considerations can be extracted. Even though ZVS conditions may be lost, as it has been stated it occurs in the non-transferring port and it is therefore not a crucial factor as losses will be negligible. Furthermore, these limits have been established for maximum power levels: it is assumable that if, for example, PV panels have a drop in their voltage, maximum power will not be demanded from it and, therefore, lower voltages can be achieved if the power from the corresponding port is not maximum. Finally, maximum voltage levels are set by the component limits and do not affect the lossless operation of the system. In particular, both ports 1 and 2 have a 150 V limit and port 3 has a 500 V limit, both LV ports set by the MOSFET limit and the HV side set by the half-bridge driver board.

4.7 Sensitivity Analysis

When building a prototype of the designed converter, not all parameters will be exactly calibrated. It is typical for components such as capacitors or inductors to have some tolerance, a range of values in the vicinity of the rated one that the component may have in reality. It is therefore important to know beforehand how will the operation of the converter be altered by these circumstances.

Two main focus will be set: the resonant tanks, including its capacitors and its inductances, and the transformer, including its magnetizing and its leakage inductances. Two different methods will be used: in the first case, as the resonant tank parameters are fixed by design, the output voltage change will be compared to the parameter change, both in percentage. In the second case however, as leakage and magnetizing inductances were taken in simulation as typical values rather than fixed, the output voltage change in percentage will be compared to the inductance value in μH. The output voltage change will be compared to the reference used during simulation, that is, 70 μH for the magnetizing inductance and 2 μH for the leakage inductance.

Firstly, the resonant tanks have been tested and the corresponding result is depicted in Figure 4.21. The graph corresponding to one parameter has been taken changing that same parameter and maintaining the other one at its nominal value. In both resonant tanks there is an important sensitivity of the output voltage to the parameter change. It is more significantly seen when the parameter is below its nominal value (a 5% decrease implies between a 25-30% increase in the voltage value, for both the inductor and the capacitor). When the parameters are higher than designed, change is still meaningful but less drastic (for the same output voltage change as in the previous case, a change of +10% in either of the two parameters would be needed).

Both resonant tanks are affected similarly and follow the same trend. In both cases, a change in the inductance value has slightly higher importance, having around a 4-5% higher effect on the voltage change in the first tank. For the second tank, this difference is lower but still the output keeps being more sensible to an inductance change (around 2-3% difference in this case). It will be of importance to keep the values of the resonant tanks as close as possible to the designed parameters.

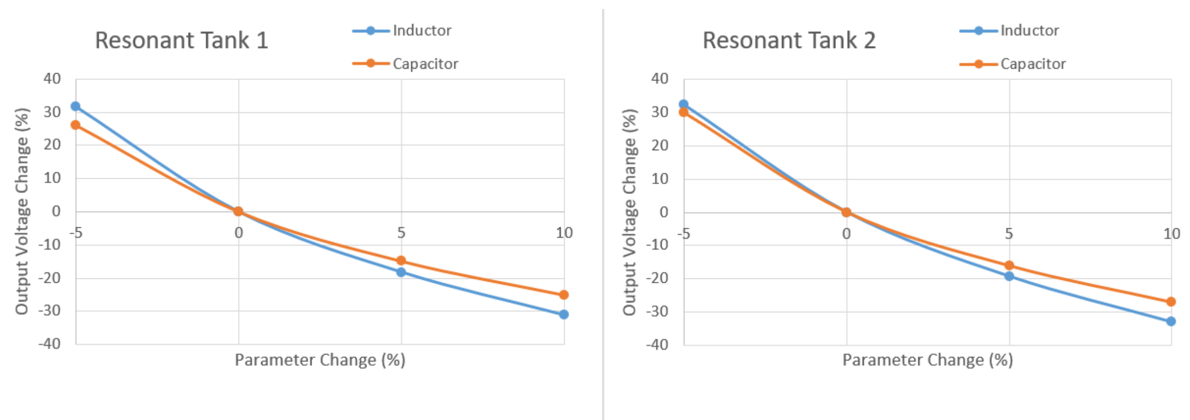

Figure 4.21: Sensitivity analysis on the resonant tank parameters.

The second test to be performed involves the transformer and the parameters in its model. The transformer to be built is expected to have different leakage and magnetizing inductances than the ones used during simulation, which were taken as in the reference article. Therefore, a study of its impact on the output of the converter is interesting to be able to know what to expect from the built model once it is known.

Figure 4.22 represents the impact of both inductances, separately, on the output voltage value. They are both referenced to the values used in simulation (which are, as stated before, 70 μH for the magnetizing inductance and 2 μH for the leakage inductance). Both inductance can have a severe impact on the output, even though in a very different way.

On the one hand, the magnetizing inductance has close to none variation on the output voltage when its value is either higher than in simulation (with only 0.1 % variation on the output for double the magnetizing inductance) or a bit lower (20 μH yield a -1% change in the output). However, change is increased exponentially when the magnetizing inductance approaches zero. Nonetheless, the magnetizing inductance does not usually decrease below that limit, and has therefore not a significant impact on the output voltage when at normal values.

On the other hand, leakage inductance presents a linear behaviour. Taking the 2 μH as the reference, doubling its value would imply a -2% change in the voltage, while tripling it has a -4% and so on. Following the same trend, reducing it to half (1 μH) would increase the output by 1%, while having no leakage would represent a 2% increase. It has therefore a more significant impact than the magnetizing inductance (considering that the latter does not go below the limit as explained before). It is however an easily predictable change as it has linear behaviour and consequently does not induce any further problems.

All in all, it can be concluded that the converter functionality is a lot more sensible to a resonant tank parameter change rather than to a change in the transformer model. However, the latter are more prone to change and cannot be designed as accurately as the tank parameters. It is therefore necessary to assess all their values when the prototype is available to test to know how will the output change, which will be a combination of all their effects.

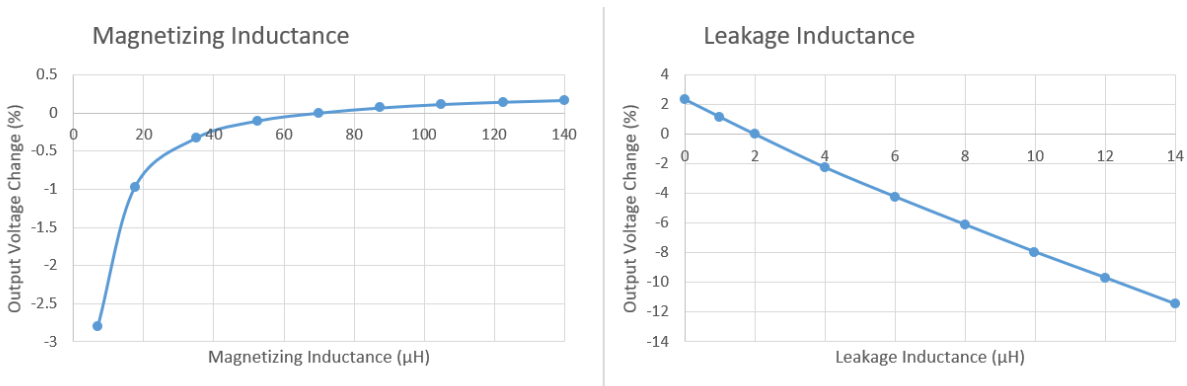

Figure 4.22: Sensitivity analysis on the magnetizing and leakage inductance values.

4.8 Efficiency Analysis

The final section based on simulation is dedicated to an efficiency analysis. It is clear that it is not possible to assess from simulation the efficiency that a prototype of the converter would have: many factors could influence its value that are not related to the design itself but rather to its 'physical attributes' (imperfectly built magnetics, cables, noise...). However, a first analysis can be performed based solely on the losses in the bridges of the converter.

As the transformer is perfectly coupled in the simulation, the only source of losses is the MOSFETs themselves (there is a contribution from the magnetizing and leakage inductances, but they will be overseen as they have already been assessed in the previous section). Even though real components will not be exactly the same as the ones used in simulation, they will have similar parameters (in particular, its $R_{ds,on}$) and it is therefore a good assessment to perform. Power levels at the input (respectively, output) of each port are taken into account to compute how much power is lost during transfer.

Table 4.3 represents all operating point, using the same definitions as in previous sections, with the power levels at each port and the computed efficiency, based on the difference between output and input power and dividing it by the input power. A negative value of power symbolizes that the port is consuming power (output power), while a positive value, on the contrary, indicates the power injections (input power).

It is observable that efficiency is high during all operation. While the first four operating points yield an efficiency higher than 98%, the last three have slightly lower efficiency, with point E being of almost 96% and F and G higher than 97%. The main difference between them is port 3: while on the first four points it is acting as the output power and is therefore consuming power, on the last two the efficiency slightly drops when the port is injecting power, and it is minimum when the port does not intervene, in operating point E.

The conclusions to be extracted are not exactly related to port 3. It is interesting to see how the lowest efficiency, point E, is achieved when power transfer between ports 1 and 2 is maximum, and it is slightly below average when port 2 has a maximum power transfer. In other words, ports 1 and 2 (low voltage high current side) have more losses than port 3 (high voltage low current side), as has been demonstrated. This is to be expected, as higher currents involve higher losses. Nonetheless, efficiency is always high and is kept satisfactorily similar during the whole operating area.

	P_1 **(W)**	P_2 **(W)**	P_3 **(W)**	η **(%)**
A	1,59	1020,50	-1005,10	98,34
B	495,69	501,49	-996,27	99,91
C	1006,40	0,72	-996,38	98,93
D	1012,00	-501,60	-495,10	98,49
E	1031,40	-988,29	0,00	95,82
F	507,16	-1005,90	520,51	97,88
G	6,95	-996,98	1018,50	97,22

Table 4.3: Power levels at each port and efficiency related to semiconductor losses.

Chapter 5

Prototyping Phase

5.1 Choice of Components

This section will introduce the prototyping phase of the converter that has been already designed, analyzed and simulated. Firstly, the choice of the components used in the prototype will be described and justified accordingly.

To build up the three full-bridges needed for the converter, different manufacturers have been consulted to verify if it is possible to get an evaluation board of an already built-in full-bridge. The main reason is to ease the building process and have a more modular approach. In case there were problems during testing, modularity is essential to quickly change the problematic component and insert the new one.

As the most probable component from the full-bridge to be broken is the MOSFET itself, it is most interesting to get the prepared board for the drivers needed to operate the bridges separately from the MOSFETs. Most solutions available from manufacturers tend to follow this indication, including room for the MOSFET to be easily soldered in without further ado. Available drivers were built for half-bridge topologies rather than full-bridge: this solution allows to connect two half-bridges to form a full-bridge and still be able to manipulate them separately in case of need. Even though in the proposed converter each bridge will be fixed at each port, two half-bridge driver boards will be purchased for each port.

The selected demonstration board for the gate drivers is the 'EVAL6494L' from STMicroelectronics. It is prepared to be used with N-channel power MOSFETs or IGBTs. It is a simple and compact board that can satisfy the needs of the prototype. One interesting differential feature is the inclusion of an adjustable deadtime through a trimmer in the form of a variable resistor. It will allow to ensure that the half-bridges at each port do not conduct at the same time at any point. The same board can be used at all ports and, therefore, six units will be used to form the three full-bridges of the converter.

The MOSFETs to be selected have to be in either the TO-220 or TO-247 package to fit the board. In all ports it is important to have an on resistance as low as possible. However, as the third port is clearly at a higher voltage (and consequently lower current) than the other two, the same component cannot be chosen for all ports.

On the low voltage side (ports 1 and 2), the selected MOSFET is 'IRFP4321PBF', from Infineon manufacturer. It stands a maximum voltage of 150 V, enough for both low voltage ports, and a maximum current of 78 A which should ensure operation at full load throughout the range of the converter (maximum currents were explored in previous sections during simulation). Its $R_{ds,on}$ is one of the lowest available, with only 15.5 $m\Omega$.

As for the high voltage side (port 3), the chosen MOSFET is 'STW28N65M2', from STMicroelectronics. It can withstand a maximum voltage of 650 V, which is a large enough security margin from the 400 V nominal voltage of the port. As for the maximum admissible current, it can withstand 20 A, which is over four times the maximum current of the port. Its $R_{ds,on}$ is 180 $m\Omega$, which ensures a low voltage drop.

To justify the adequacy of the MOSFETs and, specifically, its resistance values, a simple computation can be done. Using the maximum currents found in Table 4.2, the maximum voltage drop at the MOSFETs can be computed as shown in Equation 5.1. All ports have the maximum voltage drop at the MOSFET lower than half a volt, which is low enough for the converter design.

$$\begin{aligned} V_{drop,1} &= I_{max,1} \cdot R_{ds,on,1} = 20.33\ A \cdot 0.0155\ \Omega = 0.32\ V \\ V_{drop,2} &= I_{max,2} \cdot R_{ds,on,2} = 25.46\ A \cdot 0.0155\ \Omega = 0.39\ V \\ V_{drop,3} &= I_{max,3} \cdot R_{ds,on,3} = 2.55\ A \cdot 0.18\ \Omega = 0.46\ V \end{aligned} \tag{5.1}$$

To assemble the resonant tanks, both capacitors and inductors are needed. Regarding the latter, magnetics will be built rather than bought to be able to get the desired parameters more accurately. Design and building procedure of both inductors and the transformer will be extensively developed in the next section. Capacitors however can be bought without any complications.

Resonant tanks need to be as precise as possible to maintain its functionality. As was assessed during the previous chapter, there is a relatively high sensibility of the power transfer to a change in a tank parameter. Therefore, the best capacitors to be selected are of the C0G dielectric type. These capacitors are the most stable ones to temperature variability, as there is almost no change in their capacitance value throughout their whole temperature range. It has also close to none change within its life cycle.

These capacitors are not characterized by their maximum admissible current in their datasheet. However, a typical secure value is 3 Arms, as has been suggested by the thesis supervisor. As the maximum current through the resonant tanks are 30 A and 40 A for ports 1 and 2 respectively, values that were obtained during the voltage range analysis, there is a need to at least include 10 parallel capacitors per resonant tank.

The first resonant tank has a value of 150 nF. As 15 nF is a typical value for capacitors, 10 of these can be included in parallel. The selected capacitor is C3225C0G2J153J160AE, from TDK manufacturer. It can withstand a 630 V level (peak voltage is 450 V at the capacitance of port 1). As has been stated, 10 must be bought and put in parallel to sum up a 150 nF capacitance bank.

The second resonant tank has a value of 230 nF. As 22 nF is the closest typical value, 10 of these can be put in parallel with an extra 10 nF capacitance to form up the total value. The selected 22 nF capacitor is C1210C223KBGACTU, from KEMET manufacturer, while the 10 nF capacitor is C3225NP02J103J125AA, from TDK manufacturer. Both can withstand a 630 V value, which is lower than the 393 V maximum voltage peak that has been found during simulation.

Two filter capacitors will also be needed for the bidirectional ports 2 and 3 to correct the signals and have a DC output. Their values were computed during theoretical computations. They do not have to be as precise as the resonant tanks and therefore film capacitors are selected. For port 2, the selected capacitor is B32778P7306K000, from EPCOS manufacturer, with a capacitance of 30 μF that can withstand 700 V, far than enough for the low voltage port. As for port 3, the selected capacitor is C4AQQBW5120A3FJ, from KEMET manufacturer. It is a 12 μF capacitor rated at 1100 V, sufficient for the high voltage side of the converter.

Apart from the power stage of the converter, a controller board is needed to generate the required gate signals for each bridge. As the required control is not heavy demanding from the processors, there is a lot of suitable possibilities available from different manufacturers. One important feature is to have a fast clock speed to be able to precisely control the delay among signals and, consequently, the phase shift. It is also desirable to be able to generate all signals within one timer as all bridges switch at same frequency. A detailed analysis will be done in a later section.

The selected microcontroller is STM32F207ZG, from the STMicroelectronics manufacturer. It is already used on other applications within the CE+T company and can meet all the demanded specifications, with a clock speed of 120 MHz and advanced timers with up to 4 channels with complementary signals available. To be able to easily use and program it, a development board has been bought from the same manufacturer, with part number NUCLEO-F207ZG.

This board includes USB and Ethernet connectivity for ease of communication, and connections for all 144 pins from the microcontroller. It has also three built-in LEDs to be used and a programmable button and reset button. It can be powered via the USB cable or other external supplies of both 5 V or 3.3 V. It can also provide stable voltage outputs at the same levels to feed other components.

Prototyping boards are also needed to connect all the different components of the converter. The chosen boards are Eurocard type with inbuilt holes ready to solder in. The code of the component is RE200-LF, from Roth Elektronik manufacturer. Connectors are also needed to use in combination with the boards. Socket strips are used of code BCS-1xx-L-D-TE, where xx indicates the number of connections of the socket. More details on the number and dispositions of boards and connectors used will be included in the following chapter.

A summary of all components described in this section and in the following sections, particularly in the magnetic design and the prototype assembling, is included in Annex B. A bill of materials is formed up to perform the mentioned summary.

5.2 Magnetics Design

The first step unto the building process is the design of the magnetic components. The transformer and both inductors from the resonance tanks are to be manually built rather than bought as it will be easier to get the desired inductance values for the maximum current ratings observed in the converter.

The procedure is to be started with a theoretical computation to assess which core and winding will be used. Afterwards, when components are selected and acquired, the building process itself starts to finally finish with some tests done on the magnetics. All steps will be detailed and followed thoroughly in the next subsection. A separation has been done between transformer and inductors as the procedure presents some differences among them.

The objective is to reduce at maximum the power lost in the magnetic components. These losses will be divided into two categories, depending if they are induced by the core (core losses) or at the winding (copper losses). The former depend on the chosen core and its dimensions and the maximum flux density that will be induced, which is depending on the number of turns. It will be mathematically explored later on.

Regarding copper losses, they are directly related to Joule losses. Therefore, they depend on the resistance of the used winding and the current flowing through them. As a general approach throughout this section, worst case scenario will be always considered, that is, maximum possible current through the windings and, consequently, maximum copper losses. The sum of the copper losses at all windings and the core losses would assess the total losses of the magnetics.

Ideally, copper losses and core losses should be as close as possible. Total losses are reduced at maximum when copper losses are slightly below core losses [23]. This phenomena is illustrated in Figure 5.1, where it can be observed that the maximum flux density is proportional to the core losses and inversely proportional to the copper losses. It will be demonstrated during calculations further on. Particularly, regarding copper losses and in the case of a transformer where more than one winding is alocated, it is also of interest to maintain the different losses of the windings as close as possible not to have one winding with considerably higher losses and, therefore, increased temperature.

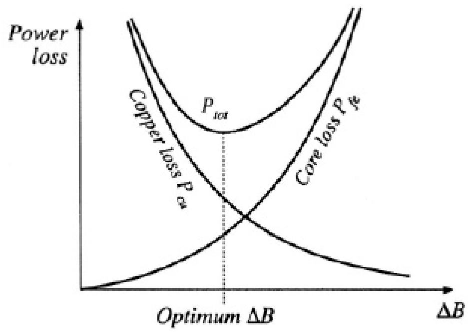

Figure 5.1: Dependence of core and copper losses on maximum flux density [23].

5.2.1 Transformer

The transformer in the designed converter includes three different windings, one per port. While two ports, and therefore two windings, are in the low voltage side, the third one is on the high voltage side. Some similarities will be assessed between the two low voltage windings: as has been seen in previous sections, they have considerably higher currents than the high voltage port.

The process of choosing the core and winding material to be used is iterative. The main goal is to be able to compute the losses in both the core and the windings and be able to minimize them under some criteria that will be further explored. To be able to show the process, only the final selected core and windings will be used in order not to excessively lengthen this section.

Transformer cores are available on different shapes and sizes. To reduce the scope of the analysis, an ETD shaped core has been recommended and consequently analyzed. Therefore, only the size of the needed core is assessed. The chosen core is the ETD49/25/16. The numbers express the nominal dimensions of the core, in mm.

Core losses depend directly on the used material. The 3C95 material from FERROXCUBE is chosen for the core at recommendation. Its main characteristic is the low variability of the losses to temperature, which allows the core to maintain its properties at different operating temperatures. Therefore, an analysis at room temperature yields similar values to an analysis at an increased temperature of 100°C, which makes it valid to neglect this difference during calculations.

To compute the core losses, firstly the peak flux density value must be computed as they are directly related. To do it, Faraday's law can be followed, which yields the following formula:

$$\hat{B} = \frac{\lambda_i}{2 \cdot N_i \cdot A_e} \tag{5.2}$$

where λ_i is the volts-second applied at winding i, N_i is the number of turns in winding i, and A_e is the cross-sectional area. The volts-second can be easily computed as the voltage applied at the transformer windings is of square shape. Therefore, it directly depends on the voltage level, the duty cycle, which is fixed at 0.5 at all ports, and the period, which is 10 μs at all ports. The cross-sectional area depends directly on the chosen core, and is 211 mm^2 for this core. The number of turns is also an unknown and has to be assessed. The computations done for port 1 is as follows:

$$\hat{B} = \frac{V_1 \cdot D \cdot T}{2 \cdot N_1 \cdot A_e} = \frac{60\ V \cdot 0,5 \cdot 10\ \mu s}{2 \cdot N_1 \cdot 211\ mm^2} \tag{5.3}$$

Different criteria influence the choice of the peak flux density and the number of turns. It is undeniable that one of the two has to be fixed to compute the other one. Here again an iterative process is to be used. While a lower flux density would induce lower core losses, it would increase the winding losses as more turns will be needed (they are proportionally inverse as can be seen from the formula).

Different number of turns have been tested and, finally, the lowest number of turns that allowed to maintain the turns ratio with the other ports as close as possible to the theoretical value has been chosen, which is 4. The peak flux density can be directly computed:

$$\hat{B} = \frac{V_1 \cdot D \cdot T}{2 \cdot N_1 \cdot A_e} = \frac{60\ V \cdot 0,5 \cdot 10\ \mu s}{2 \cdot 4 \cdot 211\ mm^2} = 177,73\ mT \tag{5.4}$$

The datasheet of the core material includes a graph in which the peak flux density is related to the core losses per cubic meter of core. If the computed value is compared on the graph, the found losses are 200 $^{kW}/_{m^3}$. Extracting the volume value from the datasheet, core losses can be directly computed:

$$P_{fe} = P_{loss} \cdot V_e = 200\ ^{kW}/_{m^3} \cdot 24100\ mm^3 = 4,82\ W \tag{5.5}$$

Once the core has been assessed, the winding has to be chosen. Taking into account the type of design and the currents that it will have to withstand, it has been recommended to use Litzwire. It is a type of multistrand wire specialized in reducing the skin and proximity losses in conductors which, as has been explained beforehand, are neglected in this calculations. As the current tends to concentrate on the outside of the wire, it includes several isolated and twisted thin wire strands aiming at having each strand be on the outside part of the wire proportionally.

Different wires are available depending on the diameter of each strand and the number contained in the wire. For simplicity purposes, only the available wires at the laboratory have been tested to assess if they could meet the design criteria. That way the availability of the wire would be immediate. As happened in the case of the core, different types have been tried but only the chosen ones will be developed to simplify the development of the section.

Firstly, it is important to know the number of turns per winding needed. As computed before, the first winding has 4 turns. Therefore, knowing the ratios established during the design phase, all winding turns are immediately obtained:

$$\begin{aligned} N_2 &= N_1 \cdot \frac{n_{23}}{n_{13}} = 4 \cdot \frac{0.12}{0.15} = 3 \text{ turns} \\ N_3 &= N_1 \cdot \frac{1}{n_{13}} = 4 \cdot \frac{1}{0.15} = 26.67 \simeq 26 \text{ turns} \end{aligned} \tag{5.6}$$

While the second winding can be perfectly related to the desired turns ratio, the third winding has to be slightly reduced to fit a natural number of turns. This will induce a higher peak flux density, resulting in higher core losses and lower copper losses. This difference however is not significant and not to be taken into account during computations.

Two different wires have been finally taken: one for the low voltage side windings (first and second), and a different one for the high voltage side winding (third). To lower copper losses at the low voltage side, as current is higher, a thicker wire is chosen, which has lower resistance. However, for the high voltage side, and consequently low current side, a smaller wire is to be used. Even though resistance is higher, the increase of losses does not overpass the benefits of having a smaller core with smaller core losses, as a thicker wire would require more window room to fit the 26 turns of the winding. Once again it is a matter of iteration, trial and compromise.

Litzwire 630*AWG41 has been chosen for the low voltage side. 630 is the number of strands that the wire fits, while AWG41 corresponds to the diameter of each strand (71 μm in the metric system). The external diameter is of 2.61 mm. For the high voltage side, Litzwire 160*AWG42 has been chosen, with 160 strand per wire and a diameter per strand of AWG42 (equivalent to 63 μm). Its external diameter is of 1.25mm. Both are available immediately in the laboratory with sufficient quantity for all windings.

The resistance of each winding must be computed. From the datasheet of the wires, its resistance per length of cable can be known. To assess the length of wire needed for each winding, the mean length per turn (MLT) has to be known. It basically represents the length of wire needed to form one turn around the core, and therefore depends directly on the dimensions of the chosen core. This is a clear example of the interconnection of the core and copper losses computation and the main reason behind its iterative nature.

Taking both values from their respective datasheets and the number of turns needed, the resistance of each winding can be easily computed:

$$\begin{aligned} R_1 &= r_o \cdot MLT \cdot N_1 = 7.5\ {}^{\Omega}\!/_{km} \cdot 85\ mm \cdot 4 \text{ turns} = 2.55\ m\Omega \\ R_2 &= r_o \cdot MLT \cdot N_2 = 7.5\ {}^{\Omega}\!/_{km} \cdot 85\ mm \cdot 3 \text{ turns} = 1.91\ m\Omega \\ R_3 &= r_o \cdot MLT \cdot N_3 = 36.29\ {}^{\Omega}\!/_{km} \cdot 85\ mm \cdot 26 \text{ turns} = 80.20\ m\Omega \end{aligned} \tag{5.7}$$

As expected, resistance of the third winding is considerably higher than in the other two windings. However, copper losses are formed by Joule losses, which means that the square of the current is the dominant factor in it. Taking the maximum currents during operation range as found in previous sections, the copper losses are as following:

$$\begin{aligned} P_{cu,1} &= I_1^2 \cdot R_1 = (30\ A)^2 \cdot 2.55\ m\Omega = 2.30\ W \\ P_{cu,2} &= I_2^2 \cdot R_2 = (40\ A)^2 \cdot 1.91\ m\Omega = 3.06\ W \\ P_{cu,3} &= I_3^2 \cdot R_3 = (4.75\ A)^2 \cdot 80.20\ m\Omega = 1.81\ W \end{aligned} \tag{5.8}$$

$$P_{cu,tot} = P_{cu,1} + P_{cu,2} + P_{cu,3} = 7.17W$$

The difference in current yields lower copper losses in the third winding even though the resistance was significantly higher. In general terms, copper losses are higher than desired and not in synchronization with core losses. The best way to reduce copper losses is to put two wires in parallel per winding. As resistance throughout the wire would be reduced by half, power losses would be consequently also reduced by half. Doing so for all windings, the final copper losses are the following:

$$P_{cu,1} = 1.15\ W \qquad P_{cu,2} = 1.53\ W \qquad P_{cu,3} = 0.91\ W \tag{5.9}$$

Total copper losses would be reduced to 3.58 W, half its value, and therefore yielding a better design. Total losses, summing up core and copper, are 8.40 W. They represent less than 1 % of the total power and are therefore considered low enough. A summary of the losses will be included at the end of this subsection. Before validating it, some computation have to be done to ensure that the design is within some limits.

Firstly, it is important to check the thermal limit of the transformer. Indeed, lost power is dissipated by the transformer resulting in an increased temperature of the system. In the worst case scenario, that is, when maximum power is lost, temperature should not be above the 100° C limit.

The estimation of the temperature rise of a transformer can be difficult to predict with precision. Assumptions and empirical conclusions are usually the means used to assess it. Generally, as heat is dissipated throughout the transformer exposed surface area, it will be dependant on both core surface area and winding surface area.

A uniformity in temperature dissipation will be assumed, without distinguishing winding or core losses. It is a logical assumption given that most of the transformer surface is formed up by the ferrite core area, which has a poor thermal conductivity [25]. Therefore, temperature will depend on the total losses and the total surface area of the transformer.

A formula relating the mentioned two variables is usually used to compute the expected temperature rise. As explained before, it has an empirical background, and therefore the relationship has been derived from real data [25]. The formula is as follows:

$$\Delta T = \left(\frac{P_{lost}\ [\text{mW}]}{A_T\ [\text{cm}^2]} \right)^{0.833} \tag{5.10}$$

While the lost power (P_{lost}) has already been computed, the surface area (A_T) must be found. It can be easily computed using the datasheet of the selected core, which includes all its dimensions. For simplicity purposes, all external core areas will be summed up except for the central region, where the winding is the most external part and the core is in no direct contact with the exterior. In that area, the winding surface will be computed as a perfect cylinder to simplify, even though overlapping exists between smaller layers.

Surface area details will not be included as they are of little interest for the development and it only consists on a geometrical characterization of the transformer. The mentioned procedure has been followed and the surface area has been established at 81.37 cm^2. Therefore, the maximum temperature increase would be:

$$\Delta T = \left(\frac{P_{lost}\ [mW]}{A_T\ [cm^2]}\right)^{0.833} = \left(\frac{8400\ mW}{81.37\ cm^2}\right)^{0.833} = 47.59\ °C \tag{5.11}$$

Given a regular ambient temperature of 20 °C, the temperature of the transformer will never be above the 100 °C limit and therefore the proposed transformer design satisfies the thermal constraint.

The final validation to be done is related to the window area of the transformer, that is, the amount of space available to fit the winding. Even if all computations up to this point successfully designate a suitable design, it will not be possible to implement it if there is too much winding for the available space. Different criteria can be used to compute the window area usage, taking into account factors such as the window utilization factor K_u, which designates the fraction of the core window that is filled with copper. Imperfections in round wire packing and insulation layers reduce this factor significantly.

Windings will be supposed to be square instead of round during window computations to assess the mentioned imperfections. Insulation layers will be put between each winding layer and between the winding and the core. Therefore, insulation layers will be always one more than the number of winding layers. The insulation will be supposed to be of 0.3 mm (defined as d_i), corresponding to the maximum thickness of the tape that will be used.

Two dimensions must be taken into account: the number of turns (large part of the core window) and the number of layers (smaller part) needed to fit, if possible, all the windings. Firstly, the longitude of all the turns in each winding is computed:

$$\begin{aligned} a_1 &= 2 \cdot N_1 \cdot d_1 = 2 \cdot 4 \text{ turns} \cdot 2.61\ mm = 20.88\ mm \\ a_2 &= 2 \cdot N_2 \cdot d_2 = 2 \cdot 3 \text{ turns} \cdot 2.61\ mm = 15.66\ mm \\ a_3 &= 2 \cdot N_3 \cdot d_3 = 2 \cdot 26 \text{ turns} \cdot 1.25\ mm = 65\ mm \end{aligned} \tag{5.12}$$

According to the datasheet, window area is 35.4 mm on the larger side of the core. While windings 1 and 2 can be fit on one layer, the third winding needs two layers. The total number of needed layers would be four. It is consequently necessary to verify if it is possible to fit the required number of layers:

$$\begin{aligned} b &= d_1 + d_2 + (2 \cdot d_3) + (5 \cdot d_i) = \\ &= 2.61\ mm + 2.61\ mm + (2 \cdot 1.25\ mm) + (5 \cdot 0.3\ mm) = 9.22\ mm \end{aligned} \tag{5.13}$$

As the available height of the core window is, according to the datasheet, 9.7 mm, all layers can be fit into the transformer. Finally, the design can be validated and the building process can be started.

The selected core ETD49/25/16 is to be bought to start the building process. Cores are usually sold by halfs to be able to introduce an air gap if needed. As for the transformer, no air gap is needed and therefore, the first step is to glue together both halfs. Silicone is used to do so. Once the core is built together, the winding process can start.

Insulation tape is to be put among all magnetic parts on the core that will be in contact with the winding. It is also a good material to be used around the core to ensure that the glue sticks both halfs together. Once the core is covered, winding can be put on it, ensuring that the insulation tape is put again between the different winding layers.

The high voltage winding will be first put as the Litzwire is thinner and, therefore, less copper will be used when winding the rest of the layers ontop. It is also physically easier to start with that winding as it has the most turns (26 per layer, counting both parallel wires). Both parallel wires will come together from one side of the core until the other side, starting there the second layer and coming back to the starting point within this new layer. The resulting winding will have both ends facing each other.

The second winding to be installed is the first port, as it has 4 turns in comparison to the 3 that the second port has. It is therefore easier to put a layer of 3 ontop of a layer of 4 than doing it the other way around. In this case, as turns do not cover the whole layer, it is preferable to put the parallel wires separately, starting one on each side of the core and coming symmetrically to the center. Indeed, magnetically speaking it is preferable to have each layer symmetrically distributed throughout the two halfs of the core.

The third winding, corresponding to the second port and having 3 turns per wire, will have a similar distribution to its predecessor. In total, four layers are put as was designed, with six connections on one side of the core (two per each of the three windings), and six more on the other side. Insulation tape can be used to ensure the reliability of the geometry and not having any of the layers fall apart.

After the transformer is built, some initial tests can be performed to model it. Firstly, an open-circuit tests will be performed on each winding to ensure that the turns ratio has been effectively set into practice. To ensure so, the inductance measured on the tests of each winding must relate within the different windings as to the squared turns ratio. Tests are performed thanks to a RCL meter and results are as follows:

$$\begin{aligned} n_{13} &= \sqrt{\frac{L_1}{L_3}} = \sqrt{\frac{32.7\ \mu H}{1.357\ mH}} = 0.155 \\ n_{23} &= \sqrt{\frac{L_2}{L_3}} = \sqrt{\frac{18.6\ \mu H}{1.357\ mH}} = 0.117 \end{aligned} \tag{5.14}$$

As the theoretical turns ratio was 0.154 and 0.115 (taking into account the approximation done on the number of turns rather than the values from simulation), it has been demonstrated that the design transformer does indeed have the expected turns ratio and the building process has been successful.

To model a three-winding transformer, five parameters are at least needed [26]. As two parameters, corresponding to the turns ratio, are already known, three more are to be found by testing the built transformer: a magnetic inductance and two leakage inductances. The former will be taken in port 1 while the other two will be taken respectively from ports 1 and 2, as to have them in series with the resonant inductances. This selection is based on getting a similar model as the one used during simulation: however, a different order of ports could be used without further problems.

The magnetizing inductance can be directly found by the open-circuit tests and has therefore already been stated: 32.7 μH. As for the leakage inductances, two tests have to be done. First, port 3 winding will be short-circuited and the RLC meter connected to port 1, obtaining the leakage inductance on port 1. Secondly, port 3 will be again short-circuited and the probe connected to port 2, obtaining the leakage inductance of port 2 . The resulting values are therefore the following:

$$\begin{aligned} L_m &= 32.7\ \mu H \\ L_{lk1} &= 0.320\ \mu H \\ L_{lk2} &= 0.193\ \mu H \end{aligned} \tag{5.15}$$

The model is therefore built and the design procedure of the transformer is finished. Figure 5.2 shows the resulting model including the five computed parameters (the turns ratio is expressed as 1:n_{13}:n_{23}).

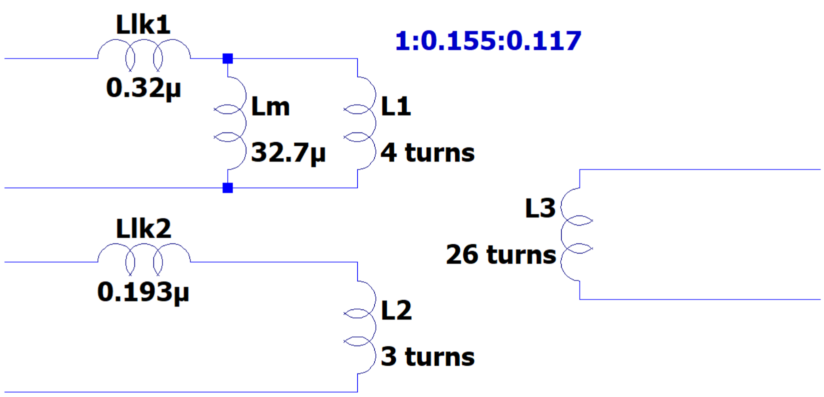

Figure 5.2: Model of the three-winding transformer.

As a final step, and once the real model of the transformer has been found, a relation with the sensitivity analysis can be performed. As it was explained during the mentioned analysis, once the difference of the magnetizing and leakage inductance from the simulation to the real data is known, the impact that it will have on the converter functionality can be known.

To assess the leakage inductance impact, both can be summed up and expressed in relation to port 3 as was done in simulation (computations will not be affected). Therefore, the value obtained during the last test can be directly taken, that is, $L_{lk,tot,3} = 28\ \mu H$. Magnetizing inductance will be taken as computed, that is, $L_m = 32.7\ \mu H$.

Magnetizing inductance value does not alter significantly the output: indeed, relating to the sensitivity analysis, change would be lower than 0.5% for any magnetizing inductance above 30 μH and below the simulation value of 70 μH.

Leakage inductance, however, is far larger than in simulation. Its behaviour when compared to the output change is linear, having a -2% change for each 2 μH added from the simulation value, which was also 2 μH. As the experimental value is 26 μH larger than the simulation value, output will be accordingly reduced by -26%. This change was to be expected as the leakage inductance taken from the reference paper was low: therefore, the percentage of change seems extraordinarily high, but it is not as meaningful as it may seem. Losses will however, as stated, influence the power transfer importantly.

A direct consequence of this change will be that the phase shift values needed experimentally will be significantly greater than the ones computed theoretically and found in simulation. The output change corresponds to worst case scenario, that is, maximum load. If tests are performed under different circumstances, lower differences are expected. However, this is a crucial factor to take into account when assessing the real meaning of the experimental phase shifts.

$$\begin{array}{llcl} L_{m,1} = 32.7\ \mu H & \text{(-53.3\% from simulation)} & \rightarrow & \text{Output change = -0.5\%} \\ L_{lk,3} = 28\ \mu H & \text{(+1300\% from simulation)} & \rightarrow & \text{Output change = -26\%} \end{array} \tag{5.16}$$

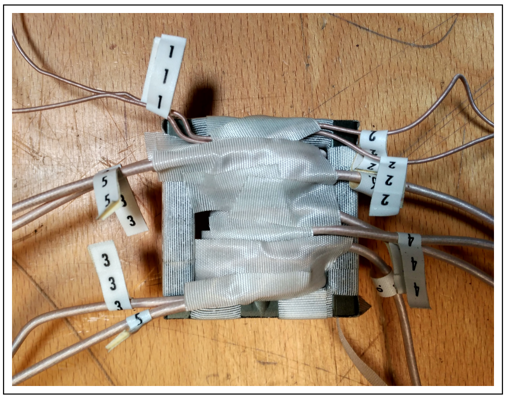

Figure 5.3: Picture of the built transformer.

5.2.2 Inductors

After the building process of the transformer is complete, the next step is to design the two inductors needed for the resonant tanks. Even though some part of the procedure will be repeated, there are other aspects to be taken into consideration in the inductors. The whole procedure will be detailed, with special focus on the new steps rather than on the ones that are repeated.

Once again, the choice of core and winding materials is iterative and can be done for as many different parts as available. Only the selected ones will be fully analyzed not to lose focus from the real objective of the section. Firstly, the core parameters will be assessed. An E-shaped core has been recommended, with the same 3C95 material as in the transformer. The optimal core that has been found is the E55/28/25. Both inductors will use the same core.

An E-shaped core is used for the inductor rather than typical toroidal cores that are becoming more and more popular in different applications. As the resonant tank current is a perfect sine wave (with a maximum variation of two times the peak current), it would have more losses in the toroidal core, which is better for other purposes such as power supplies (inverters). On the contrary, the ferrite E core would not be able to work in an inverter as it would get too hot quickly.

The computation of the number of turns needed is related to the peak flux density, as was seen in the previous subsection. Their inverse relationship is, in this case, also complemented by two new factors that must be taken into consideration: air gap length l_g and inductance value L. The following two formulas establish the relationship between these variables:

$$\begin{aligned} l_g &= \frac{\mu_0 \cdot L \cdot I_{max}^2}{\hat{B}^2 \cdot A_c} \\ N &= \frac{L \cdot I_{max}}{\hat{B} \cdot A_c} \end{aligned} \tag{5.17}$$

where l_g is the air gap length of the inductor, in m; μ_0 is the vacuum permeability, a constant of value $4\pi \cdot 10^{-7}$ H/m; L is the desired inductance value, in H; I_{max} is the maximum current, in A; $\hat{B}$ is the peak flux density, in T; A_c is the core cross-sectional area, in m^2; and N is the number of turns.

As the maximum current is fixed by the converter operation, the inductance value is fixed by design and the cross-sectional area is fixed by the chosen core, only three variables remain. One of them must be set in order to find the other two. The peak flux density will be fixed, taken into account that it is directly related to the core losses as was seen in the previous subsection.

Indeed, looking at the datasheet of the selected core material, peak flux density and core losses per unit of volume are directly correlated. Once again this is an iterative process in which different values for peak flux density can be tested to see how the whole inductor behaves. After some iterations were made, a suitable peak flux density was found to be 0.15 T for both inductors. Its value is below the saturation point of the material, which is established at 0.32 T. Its corresponding core losses, according to the datasheet, are $P_{loss} = 100\ {}^{kW}/_{m^3}$. Obtaining the volume value of the core also from the datasheet, core losses would be:

$$P_{fe} = P_{loss} \cdot V_e = 100\ {}^{kW}/_{m^3} \cdot 52000\ mm^3 = 5.20\ W \tag{5.18}$$

Going back to the air gap length and number of turns computation, and once the peak flux density has been established, both values can be directly found. As a reminder, the desired inductance values are $L_1 = 20.43\ \mu H$ and $L_2 = 13.08\ \mu H$ for resonant tanks 1 and 2, respectively. Moreover, their peak current as was found during the voltage range analysis is, respectively, $I_{max,1} = 42\ A$ and $I_{max,2} = 55\ A$.

The cross-sectional area of the core, according to its datasheet, is $A_c = 420\ mm^2$. Each one of the inductors has a different value of air gap length and number of turns, according to their inductance value and peak current. The procedure, taking back the formulas exposed before, is the following:

$$\begin{aligned} l_{g1} &= \frac{4\pi \cdot 10^{-7}\ {}^{H}/_{m} \cdot 20.43\ \mu H \cdot (42\ A)^2}{(0.15\ T)^2 \cdot (420 \cdot 10^{-6})\ m^2} = 4.37 \cdot 10^{-3}\ m = 4.37\ mm \\ N_1 &= \frac{20.43\ \mu H \cdot 42\ A}{0.15\ T \cdot (420 \cdot 10^{-6})\ m^2} = 13.62 \text{ turns} \simeq 13 \text{ turns} \end{aligned} \tag{5.19}$$

$$\begin{aligned} l_{g2} &= \frac{4\pi \cdot 10^{-7}\ {}^{H}/_{m} \cdot 13.08\ \mu H \cdot (55\ A)^2}{(0.15\ T)^2 \cdot (420 \cdot 10^{-6})\ m^2} = 4.88 \cdot 10^{-3}\ m = 4.88\ mm \\ N_2 &= \frac{13.08\ \mu H \cdot 55\ A}{0.15\ T \cdot (420 \cdot 10^{-6})\ m^2} = 11.42 \text{ turns} \simeq 11 \text{ turns} \end{aligned} \tag{5.20}$$

The number of turns has been approximated to its immediate lower natural number. This approximation will imply slightly higher core losses (as peak flux density and number of turns are inversely proportional) and lower copper losses (as less winding will be used). Nonetheless, this changes are not significant and they can be neglected (further computations will be done with the natural number of turns, as it will be the real value used during the building process). Air gap length is similar between the two inductors and, in any case, of realizable size. Its value will be further explored during the building process.

Once the air gap length and number of turns are defined, the copper losses can be assessed. The wire choice is again based on iteration among different types. However, in this case, to ease the prototyping process, the same wire type as in the transformer will be used. As a reminder, the chosen wire is Litzwire 630*AWG41, with 630 strands of 71 μm each, an exterior diameter of 2.61 mm and a resistance of 7.5 Ω/km, for both ports 1 and 2.

Copper losses computation uses the same procedure as in the transformer case. Knowing that the Mean Length Turn (MLT) of the core is 100 mm, the resistance of each inductor can be computed:

$$\begin{aligned} R_1 = r_o \cdot MLT \cdot N_1 = 7.5\ \Omega/km \cdot 100\ mm \cdot 13 \text{ turns} = 9.75\ m\Omega \\ R_2 = r_o \cdot MLT \cdot N_2 = 7.5\ \Omega/km \cdot 100\ mm \cdot 11 \text{ turns} = 8.25\ m\Omega \end{aligned} \tag{5.21}$$

As copper losses are formed up by Joule losses, apart from the wire resistance only the rms current is needed. As was found during simulation, and used at the transformer computations, the maximum rms current for ports 1 and 2 are $I_1 = 30\ A$ and $I_2 = 40\ A$ respectively. It is worth noting that, in this case, rms current is used, rather than peak current, as was the case during the air gap length and number of turns calculations. Copper losses are therefore:

$$\begin{aligned} P_{cu,1} = I_1^2 \cdot R_1 = (30\ A)^2 \cdot 9.75\ m\Omega = 8.78\ W \\ P_{cu,2} = I_2^2 \cdot R_2 = (40\ A)^2 \cdot 8.25\ m\Omega = 13.20\ W \end{aligned} \tag{5.22}$$

To reduce losses, the same procedure as in the transformer case will be used: two wires will be placed in parallel in both the inductors. Copper losses will be consequently reduced by half. The losses per each inductance are finally as follows:

$$\begin{aligned} &P_{fe,1} = 5.20\ W \qquad &&P_{fe,2} = 5.20\ W \\ &P_{cu,1} = 4.39\ W \qquad &&P_{cu,2} = 6.60\ W \\ \\ &P_{tot,1} = 9.59\ W \qquad &&P_{tot,2} = 11.80\ W \end{aligned} \tag{5.23}$$

Final losses are slightly higher than in the transformer (which were 8.40 W), but they are still low enough to consider them viable for the prototype (they represent each around 1% of the maximum power). Once again, these are worst case scenario losses, that is, the maximum losses that could theoretically be found in the inductor. Actual losses should be lower than the computed value, even though some aspects (i.e. proximity losses) have been neglected and they could consequently produce higher losses. Core and copper losses are also similar in both inductors, which, as was explored at the beginning of the section, is a sign of reduction of overall losses and an efficient design.

Validations need to be done for the inductors as it was the case for the transformer. First, the thermal limit will be checked. Once again the same empirical formula as in the previous subsection will be used, with the losses that have been just computed and the surface area in contact with the exterior, which is a geometrical characterization using the dimensions available in the datasheet of the core as well as the winding expected surface, taken as a perfect cylinder:

$$\begin{aligned} \Delta T_1 &= \left(\frac{P_{tot,1}\ [mW]}{A_T\ [cm^2]}\right)^{0.833} = \left(\frac{9590\ mW}{107.61\ cm^2}\right)^{0.833} = 42.09\ ^\circ C \\ \Delta T_2 &= \left(\frac{P_{tot,2}\ [mW]}{A_T\ [cm^2]}\right)^{0.833} = \left(\frac{11800\ mW}{107.61\ cm^2}\right)^{0.833} = 50.04\ ^\circ C \end{aligned} \tag{5.24}$$

Both temperature increases are similar to the previously computed for the transformer (which was 47.59°C), which makes the design valid from the thermal point of view: temperatures are in equilibrium throughout the magnetics and far from the 100 °C limit at room temperature).

Second limit to be checked is the window area availability. Once again wires will be taken as square to easily assess the imperfections in the window utilization factor. Moreover, there has to be some margin between wire usage and window area as the core is E-shaped and winding will not be as tightly fixed as with the round-shaped central area of the ETD.

Starting with the wider part, that is, the number of turns assessment, the following values are computed:

$$\begin{aligned} a_1 &= 2 \cdot N_1 \cdot d_1 = 2 \cdot 13 \text{ turns} \cdot 2.61\ mm = 67.86\ mm \\ a_2 &= 2 \cdot N_2 \cdot d_2 = 2 \cdot 11 \text{ turns} \cdot 2.61\ mm = 57.42\ mm \end{aligned} \tag{5.25}$$

Given that, according to the datasheet of the core, the measurement of the window along the central region surface is 37 mm, two layers will be needed for both the inductors. Lastly, it is necessary to assess if the core window is capable of having two layers of winding, taking into account that the insulation tape has to be once more put between layers and between core and layer. Using the same insulation thickness as in the transformer case (0.3 mm per layer), the following computation is performed:

$$\begin{aligned} b_1 &= 2 \cdot d_1 + 3 \cdot d_i = 2 \cdot 2.61\ mm + 3 \cdot 0.3\ mm = 6.12\ mm \\ b_2 &= 2 \cdot d_2 + 3 \cdot d_i = 2 \cdot 2.61\ mm + 3 \cdot 0.3\ mm = 6.12\ mm \end{aligned} \tag{5.26}$$

According to the datasheet, the available window height is 10.15 mm. Therefore, both inductors can have their respective windings in their available window area with a large enough security margin, which assesses for the E-shaped imperfections.

Once the design has been validated, the building process can be started. As the same core is used, four halfs will be bought. In the inductor case, as an air gap is needed, the first step will not be gluing together the two halfs but rather mounting the winding in the separated core. Even though air gap length has been computed, it is better procedure to use an RLC meter and measure the needed length experimentally to get as close as possible to the theoretical value.

As two wires are placed in parallel, each one of them will start from each core half, from the side the most separated from the air gap. It is prefarable to avoid having further losses by placing winding as far away as possible from the air gap area and its surroundings. Therefore, a first layer of 7 turns (6 for the second inductor) will be placed, and a second layer of 6 turns (5, respectively) will be put on top, returning to the starting position and going out on the opposite direction as it has gone in. Both wires in the same inductor will be completely symmetrical, as it is preferable to avoid larger losses.

It is important not to forget the crucial part that the insulation tape has in this process: before the winding placement, it has to be put on every core part that will be in contact with the winding and, later, between layers. It can also be used at need to ensure the robustness of the winding configuration, as far as the available window area allows to do so. Indeed, in the real configuration, layers do not have a large margin inside the window area as opposed to the theoretical computations, which implied that half the window would be empty. As was to be expected, the E-shaped core (with a squared central region) does not accommodate the winding as tight as in the transformer case. Nonetheless, everything can be fit without further problems.

Once the winding is fixed, the air gap length computation can be started. Several plastic pieces have been cut down and shaped so that they can be placed between the physically in contact parts of the two halfs. Each spacer is 2 mm thick: if further precision would be needed, thinner spacers could be used in conjunction. An RLC meter has been used and different spacers have been placed one by one between the two halfs to assess the inductance value. As glue between them will make the air gap slightly higher, it is important to take a higher value of inductance rather than a lower one as the inductance will tend to decrease a bit.

The first inductance has needed 3 spacers placed to achieve an inductance of 21 μH, 2.8% higher than the theoretical value. In the case of the second inductance, 5 spacers have been needed to achieve an inductance of 13.40 μH, 2.5% higher than the theoretical one. The number of spacers is translated into an air gap length of 6 mm for the first inductor and 10 mm for the second inductor.

Air gap length is considerably higher than in the theoretical computation, which implies that it was a good idea to assess experimentally its real value rather than just sticking to the computed one. It is not however an important difference, as the inductance value has been achieved and there is no further consequences for this change. After gluing the core halves with the spacers and letting it dry out, the values shown in Equation 5.27 are the final ones obtained, slightly lower than the previous ones as was to be expected.

Finally, deviation from the designed values can be related to the sensibility analysis performed during simulations. Indeed, as was the case with the transformer model, the analysis can predict how will the output of the converter change knowing the parameter change in the resonant tanks. As was seen in its subsection, there is a large sensitivity, which is the main reason why the experimental value has been kept as close as possible to the designed one.

$$\begin{aligned} L_1 &= 20.65\ \mu H \quad (+1.07\ \%\text{ from design}) \\ L_2 &= 13.30\ \mu H \quad (+1.68\ \%\text{ from design}) \end{aligned} \tag{5.27}$$

A +5% change in the inductance value was translated into a -18.21% change in the output for the first inductor and -19.33% change for the second one. Even though relation is not completely linear, it can be approximated as if it was, yielding the following output changes:

$$\begin{aligned} \Delta V_{o1} &= +1.07\ \% \cdot \frac{-18.21\ \%}{+5\%} = -3.90\ \% \\ \Delta V_{o2} &= +1.68\ \% \cdot \frac{-19.33\ \%}{+5\ \%} = -6.49\ \% \end{aligned} \tag{5.28}$$

Even though parameters have been kept closely related to the theoretical ones (typical inductance tolerance from commercial components is ±5 %, far higher than the obtained deviation), output change cannot be neglected. This change, along with the transformer model deviation and the capacitor tank, which will be computed in a future subsection, will have to be taken into account during experimental validation. Once again, deviation is computed under worst case scenario, which means that deviation may be not as important as computed if the converter is tested under non-extreme conditions.

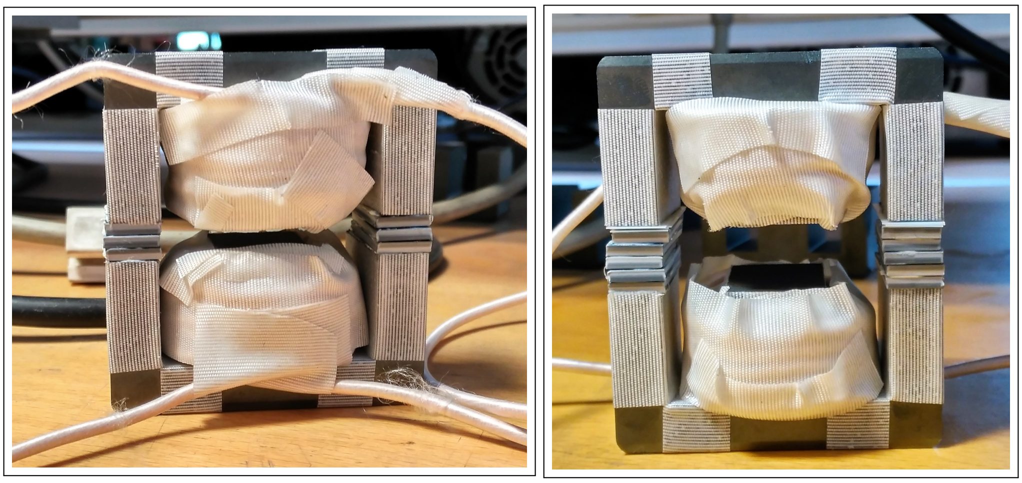

Figure 5.4: Picture of the built inductors for port 1 (left) and port 2 (right).

5.3 Microcontroller Programming

Control stage is an essential part of the converter prototyping process. It represents the interconnection between the power stage (the converter itself) and the user. Definition of a control strategy will establish how the converter will work. Its correct programming and definition is therefore of paramount importance to have the converter functionality as expected.

The microcontroller must be programmed so that six control signals, one per half bridge, will be generated. They will be gathered together into three pairs of complementary signals (one per full-bridge), which have to be able to be phase-shifted at will. All signals will have the same frequency (100 kHz, the switching frequency) and a fixed duty cycle of 50%. No deadtime is needed between the complementary pairs as the half-bridge boards used in the prototype already implement a manually-set deadtime. Moreover, as only one control signal is introduced per half-bridge, a software-induced deadtime would only delay the half-bridge between themselves, rather than avoid a short-circuit among one half-bridge which is the purpose of deadtime.

To generate periodic signals, at least one timer must be used. As their name suggests, they are able to count time steps and trigger events at a desired moment, depending on the configuration in which they are programmed. The microcontroller also features an internal clock, which is the base that timers use to count time in synchronization with it. Timers are able to count either in parallel with the clock speed or at a slower ratio, jumping through several clock ticks, but they can never go quicker than their related clock.

The STM32F207 microcontroller was the chosen component for the control stage. It has been bought built in a development kit, with part number NUCLEO-F207ZG, allowing for easy communication with a PC host to program it and featuring several input/output pins to connect with every pin from the microcontroller itself. The STM32 family can be programmed through manufacturer software, called STM32CubeMX, which allows to easily select the pins to be used, its modes and the main variables.

The selected component features a total of 14 different timers. Two of them, defined as advanced timers, have four output channels each available, with their respective complementary channel. The rest of timers, defined as general purpose timers, feature different characteristics, but none of them has complementary outputs. As this feature is a real need for the application, an advanced timer will be used. All signals run on the same frequency, which implies that no more than one timer is needed to generate all signals.

TIM1, the chosen advanced timer, can set its counting speed up to the same frequency as the controller clock, which is 120 MHz. It can be configured into four different modes: input capture, PWM generation, forced output and output compare. The first mode has the ability to measure the moment at which an input signal is obtained and store that value to use at will. PWM generation sets a pulse signal that can be modulated and its duty cycle changed, as its name suggests. In forced output mode, the pin level can be established at the desired level, forcing it to stay in that level.

The last mode, output compare, is the one that is of interest for the application and consequently the one in which the timer will be configured. In this mode, a preset register value is compared to the counter of the timer. When both register match, some event can be triggered. This mode allows to create periodic signals of fixed duty ratio: indeed, the mode can be configured to toggle the signal at match. Therefore, if the timer is set to count at double the speed of the signal frequency, the signal can be turned on or off at the fixed moment periodically, creating a signal of 50% duty cycle.

Moreover, the registry of each signal can be set at will allowing to create shifted signals. It therefore includes all the requirements that the application needs. Phase-shift will be able to be modified by just changing the comparison register. Timer will be configured to have three outputs active (with its complementary signals) in output compare mode, under the toggle on match configuration.

After selecting the timer to be used, its outputs and the mode, three parameters must be defined to finalize its configuration. These are the prescaler (PSC), the autoreload register (ARR) and the capture/compare register (CCR). The first two will be fixed and established at the timer level, that is, all outputs will have the same register value. The third one will be variable and established differently for each output, as it will relate to the phase-shift of its signal.

The PSC is used to slow down the clock frequency. Its register value symbolizes the integer that the clock will be divided to. For example, a prescaler set at two will divide by two the clock frequency. In the case of the timer in use, it would get the clock down to 60 MHz from the 120 MHz of the internal frequency. Its main purpose is to avoid overflow in some application: high clock rates will overflow the timer quicker. It is also known as counter divider.

For this application, no counter divider is desired as it is of interest to have as many time steps as possible per period. Indeed, the more steps there are, the more precision can be obtained for the phase-shift computation. PSC will be therefore set at the minimum value, that is, 1 (register will have to be set at 0, as it is the starting bit which would imply no division in the counter).

The ARR sets the number of clock ticks at which the counter will be reset. In other words, it sets the frequency of the output signal. If, for example, ARR is set as 10, the output signal will have a frequency of 12 MHz, as steps are at clock speed of 120 MHz. The register is set as a 16-bit value, which implies that for some applications in which frequency has to be further lowered, the PSC would play a key role in conjunction.

As the desired switching frequency is 100 kHz, the counter has to be at double its speed to be able to set both on and off the switching signal per period. A simple computation can be done to establish the needed ARR register value:

$$ARR = \frac{120\ MHz}{2 \cdot 100\ kHz} = 600 \tag{5.29}$$

The ARR register will be therefore set at 600 (register-wise, its value is 599, as it starts counting from zero). Practically, it would mean that the counter is reset each 600 clock ticks. As the counter period accounts for a maximum phase shift of 180° (as the period is double when compared to switching signal), it is possible to assess how precisely the phase-shift will be able to be set.

Lastly, the CCR must be set separately per each output signal. Its register will be compared to the counter and, when there is a match, the output signal will be toggled. Its value has to be therefore set between 0 and 599, as it has to be related to the ARR value. Regarding phase shift precision, it can be easily computed how would one clock tick difference relate to phase shift change:

$$\Delta\phi = \frac{180^\circ}{600 \text{ steps}} = 0.3 \ {}^\circ\!/\text{step} \tag{5.30}$$

Precision is low enough to be able to compare the experimental results to the simulations. During simulation, control voltage sources were delayed with a precision of 0.01 μs, which corresponds to 0.36° (as the period is 10 μs, corresponding to a 360° shift). Consequently, experimental phase shift precision is closely related to the used during simulation, which is desirable to establish the required comparisons.

Once the two first registers are established through the SM32Cube software, the output pins can be assigned. Each signal has several pins available for the user to select them. The six pins needed for all signals are selected close together for simplicity purposes, and specifically on pins PE_8 through PE_13 from the development board. Once the pins are selected, the software allows to generate the code to be opened in a code compiler. MDK-ARM V5 is used for that purpose.

Some modifications have to be introduced in the code manually before compiling it to the board. The timer channels have to be manually initialized through the initialization function already introduced in the code (both the regular and complementary outputs must be initialized). A pointer to the timer in use and a name specification of the channel are demanded by the function.

Moreover, a small conversion code can be written to easily introduce the desired phase shifts. Channel 1, corresponding to port 1, will have its CCR set at 0 as it is the reference. For channels 2 and 3, the phase shift is introduced and a conversion is performed to establish which CCR value corresponds to that phase shift, following the same procedure as used before.

It is of interest to also include some control loops: phase shift 1-3 has to be between 0° and 90° while phase shift 1-2 can have a value between -90° and 180° (as was seen during theoretical computation, as phase shift 1-2 does not directly relate to a power transfer). If phase shift 1-2 has a negative value, CCR of port 1 has to be modified to change the reference accordingly, as the registry cannot go below zero.

The complete code, including the final additions, is included in the annex. Once the code is finalized, it can be compiled into the microcontroller board for testing purposes. To observe if the generated signals are indeed as expected, a PicoScope tester is used. Each one of the six designated pins can be seen through a probe to verify if the signals are as expected. The board itself is provisioned with several ground pins for the probes to correctly check the voltage levels of the output signals.

Figure 5.5 depicts the three main output signals. They would correspond to a half-bridge of each port. CCR values have been established at 0, 199 and 399 respectively, creating a reference signal (blue) for port 1, a 60° phase-shifted signal (red) for port 2 and a 120° phase-shifted signal (green) for port 3. These value are just for testing purposes and do not correspond to any concrete operating point. As can be seen, phase-shift is correctly established throughout the signals. Moreover, they all have the same period of 10 μs and its duty cycle is 50%. Signals are 3.3 V when set, as expected for control purposes.

Figure 5.6 shows a pair of complementary signals. All three pairs of signals are exactly equal when compared: each complementary signal has opposite polarity to its pair, being set when the other is reset and vice versa. Signals are therefore being generated as expected and the control programming has been successful.

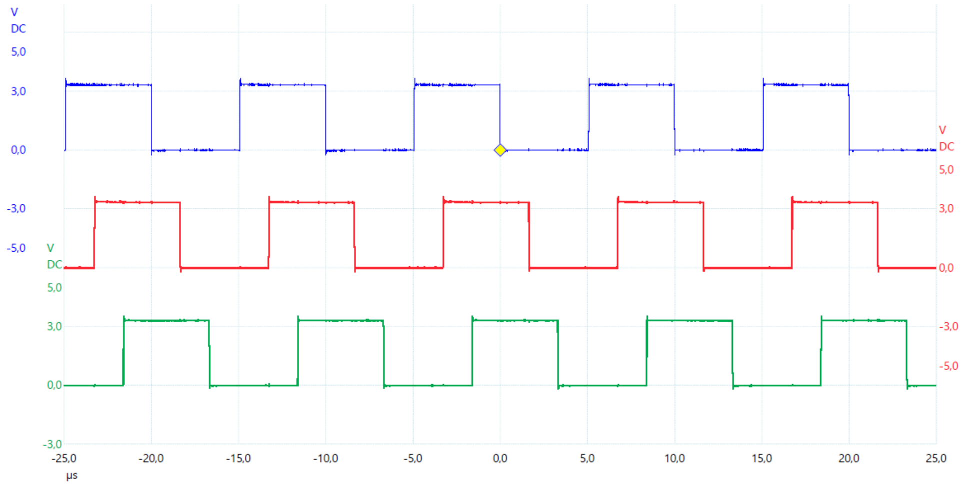

Figure 5.5: Three main signals of the controller phase-shifted 60° and 120°.

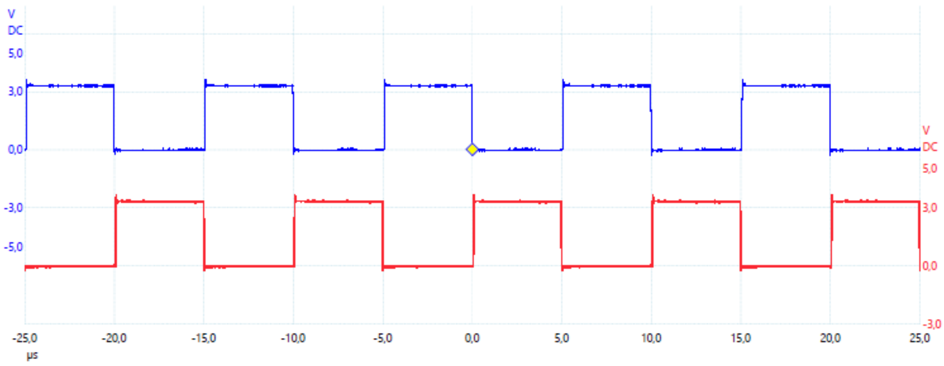

Figure 5.6: Pair of complementary signals of the controller.

5.4 Prototype Assembling

Once all components have been chosen, magnetics have been built and the controller has been programmed, the prototype is ready to be assembled. An overview of the different component connections will be done, aiming at justifying all the choices made during the prototype design.

Firstly, the half-bridge board adaptation will be assessed. As was introduced during the choice of components, boards are built to fit external MOSFETs. Therefore, first step is to solder the MOSFETs in its respective pins. Board has several connections that allow to have several inputs and outputs. They are the following:

- IN: Input for the control signal. It must be connected to the controller board pin that corresponds to the selected half-bridge.
- SD: Shutdown pin, it disconnects the bridge if the pin is forced low. No need for the prototyping and testing processes.
- Vpu: 5 V signal that feeds the SD pin among other parts of the driver. When the bridge is fed, this port is automatically set at its voltage level.
- Vcc: Source signal to be fed to have the bridge operating. It is recommended, according to datasheet, to be set between 10 and 20 V.
- SGND: Grounding for the control signal side.
- HV: High voltage power pin, it must be fed with the positive side of the DC voltage of each port.
- OUT: Power pin that corresponds to the point between both MOSFETs of the same half-bridge. It will be connected to the resonant tanks and, consequently, the transformer.
- PGND: Grounding for the power part.

The IN and SGND pins will be connected to the microcontroller board. While the SGND will be equal for the six bridge boards, the IN pins will be connected to each one of the signal pins as explained during the last subsection. The Vcc pin will be fed by a 12-V inverter. Its positive side will be connected to all six bridges equally, while the negative will be connected to the PGND side of each bridge. The HV and PGND of each pair of half-bridges will be connected to their respective port source or load.

The OUT pin of each half-bridge will be connected to the power stage of the converter. For ports 1 and 2, one of the bridges OUT pin will be connected to the resonant tank and the transformer winding in series. The other side of the transformer winding will be connected to the other OUT pin of each pair of half-bridges. For port 3, as no resonant tank is present, the OUT pins are directly connected to the transformer windings. After this, all pins from the bridge boards have been connected successfully.

The microcontroller board will be fixed in a prototyping board to have a more stable base and have more flexibility in transportation. It will be firstly fed via USB by connecting it to a laptop, from which the programming will be built unto. There is also the possibility of using an external supply to power it once the programming is built, by either a 3.3V, 5V or 7-12V source.

On the power stage (resonant tanks and transformer), a prototyping board will be used. All magnetics, capacitor tanks and connections to the OUT pins of the bridges will be gathered together in one board. Copper adhesive tape will be used on top of the prototyping board to effectively connect all components. To organize it, a differentiation is made between ports 1 and 2 and port 3.

For ports 1 and 2, four different equipotential areas are defined. First area is connected to one of the OUT pins and the capacitor tanks. Second area merges the other side of the capacitor tank and the inductor. A third area includes the other side of the inductor and the transformer winding, while the fourth one connects the other side of the transformer winding with the OUT pin of the second half-bridge of the port.

For port 3, even though no resonant tank is present, it has been suggested for security reasons that a capacitor should be included in series to decrease transient spikes during switching. This capacitor has to be at least an order of magnitude larger than the resonant capacitors not to interfere in its functionality (at least 2 μF), and it will have a voltage drop of less than a volt. Therefore, three equipotential areas are defined: from one OUT pin to the capacitor, from the other end of the capacitor to the transformer winding, and lastly from the other winding end to the second OUT pin.

All connections are done with Litzwire as was the case with both the transformer and the inductors. For the AC side (power stage), it is preferable to use this kind of cable for the same reasoning as in the magnetics case. Cables are soldered to the copper tapes and fixed to the board for robustness with a metallic strip. It is important to maintain a few millimetres distance between copper tapes to avoid arcing. Litzwire cable has also to be covered with insulation tape when it could get in contact with other conductive parts as isolation is not efficient.

Litzwire connection cables will be spun throughout the power stage. The objective is to reduce the noise among them and therefore reduce its losses and interference within the signals. Wires will be spun with their respective grounds, as well as parallel wires in the case of the magnetics. It is also of interest throughout the converter to reduce the cabling length at maximum, as larger current loops could also induce higher losses and noise. Once the power and control stages have been fixed and connected, the connection with the ports has to be established, that is, source and load connection as well as filtering capacitors. They will be fixed in another prototyping board. Screwed-in connectors will be used to set the cabling from the respective source or load. From there, for the bidirectional ports (ports 2 and 3), the filter capacitor will be put in parallel to the source and cabling will go out to the HV and PGND ports of each respective bridge. A thicker cable will be used for ports 1 and 2 as more current is expected than in port 3. Nonetheless, regular cables can be used instead of Litzwire.

Once the prototype is completed, first test to be done is the assessment of the real value of the capacitance tanks. A link to the sensibility analysis can be established to see how the output of the converter will be affected by the deviation of the capacitance value. An RLC meter is again used, which yields the following values:

$$\begin{aligned} C_1 &= 151.8\ nF \quad (+1.20\ \%\text{ from design}) \\ C_2 &= 232.8\ nF \quad (+1.22\ \%\text{ from design}) \end{aligned} \tag{5.31}$$

Deviation is almost the same as in the inductance case. As they were manually built and the capacitors were bought, it can be established that the deviation obtained at the inductors is indeed a good value. Sensibility analysis yielded similar results for the inductor and the capacitance; once again its trend can be taken as linear and computed:

$$\begin{aligned} \Delta V_{o1} &= +1.20\ \% \cdot \frac{-14.89\ \%}{+5\%} = -3.57\ \% \\ \Delta V_{o2} &= +1.22\ \% \cdot \frac{-16.13\ \%}{+5\ \%} = -3.94\ \% \end{aligned} \tag{5.32}$$

As deviation in the inductances were -3.90 % and -6.49 % for ports 1 and 2 respectively, the output change due to the resonant tank parameters is of -7.47 % for port 1 and -10.43 % for port 2. This phenomena implies that phase shifts will have to be greater during the experimental phase to counteract it. It is important not to forget the deviation computed from the leakage inductance of the transformer, which was of -26 % and is of course not negligible.

The prototype is expected to need higher phase shifts overall its operational region to achieve the same power levels as in simulation. It is expected that other components of the converter, as well as cables and connections themselves, will also increase somewhat the overall losses. All these imperfections should not however change the functionality itself of the converter. Indeed, it is expected that the prototype will be able to achieve all the operating points while maintaining its lossless switching operation.

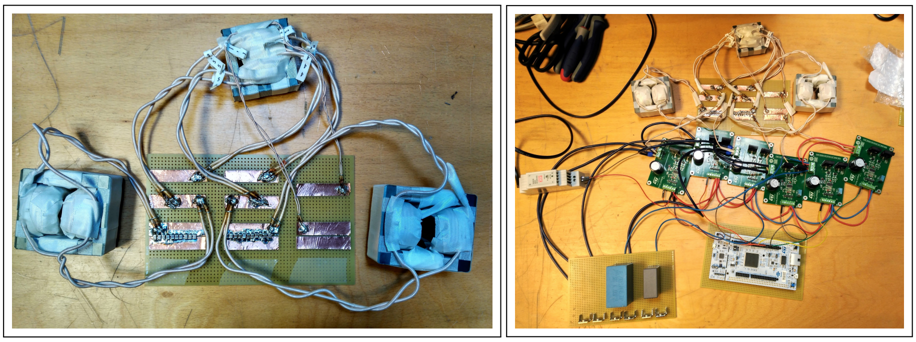

Figure 5.7: Picture of the power stage (left) and of all the assembled prototype (right).

Chapter 6

Testing Phase

6.1 Source Preparation

Finally, once the prototype has been built, an experimental validation is to be performed to assess its functionality. Tests are to be prepared to verify if the theoretical and simulation analysis correspond to reality and if indeed the prototype is operational. Different steps are to be followed to do an structured analysis and try to unravel the different characteristics of the experimental results.

First section is dedicated to the source preparation. Even though the purpose of the converter has been mentioned in several occasions (PV panels, battery and distribution), initial test to be performed on the prototype will not feature directly this sources but rather a laboratory simulation of them. The different equipment in use will be presented to understand how their functionality is characterized.

Port 1 represents an unidirectional port, as PV panels will never consume power. Therefore, only a rectifier is needed to feed the 60 V level unto the converter. It should be able to withstand at least 42 A of current, as it is the peak maximum current for that port, as was computed in previous sections. PV panels are supposed to have larger variability in its VI curve, however, for testing purposes, constant operation is to be expected.

A rectifier from the ascom brand is to be used during experimentation. It is fed by regular 230 V AC input and it is able to deliver an output between 40 and 60 V DC. Moreover, it can generate a current of up to 70 A, being able to regulate it and limit it down to 10 A. The theoretical maximum power would therefore be 4.2 kW, more than enough for the 1 kW maximum power of the converter.

However, on a first stage, lower power will be used to securely assess the prototype functionality. On that purpose, a laboratory power supply will be used. The model is POWERLAB 605D-II, which includes two independent power sources that can be also used in series or parallel. Each source can deliver a voltage range of 0-60 V and a current output of 0-5 A, making it possible to achieve a 0-120 V range when in parallel and a 0-10 A range when in series.

The maximum deliverable power at 60 V operation (connecting both sources in series) would be 600 W. It is therefore a really interesting intermediate solution to reliably test the operation of the converter at low power. Moreover, the supply can work in either constant current or constant voltage mode, supplying a stable system nonetheless of the mode in use. It can also be used for first tests on either of the ports, or even separately in two ports at the same time.

Port 2 represents the battery storage system, and it is therefore a bidirectional port. A real battery is not recommended to be used when testing the functionality as its level is not stable. It is preferable therefore to use another rectifier at the 48 V level. In parallel, a load system is to be used. In conjunction, they can withstand both the generating and consuming functions of the port. The load must be able to be regulated at will to test the different operating points of the converter.

The rectifier in use for this port will be from Automation manufacturer, with part number HPSM-48-30. The input is a regular 230 V AC supply, whereas the output sets a 48 V stable signal. Its maximum current is 30 A, which translates into a maximum power of 1.4 kW, enough for a full test of the converter capability. The voltage level can be tuned within a small margin for voltage range analysis.

The load bank to be used is a custom bank present at the company. It has up to 8 loads in parallel that can be connected or disconnected at will. The maximum applicable voltage is 60 V, however, at the rated voltage of 48 V for the port, each load represents a power of 280 W (its resistance is 8.2 Ω). Connecting all loads, the maximum power at 48 V would be 2.2 kW, and therefore being sufficient for the converter rated power. Each load is protected by a circuit breaker of 16 A.

Port 3 represents the distribution side, and, as was justified during the design phase, it is also meant to be bidirectional. Its level is 400 V, and it is therefore a bit trickier to obtain with lab equipment when compared to the other two low voltage side ports. In first tests, only the two first ports will be used to simplify the testing process and obtain first results. Once that is achieved, the third port can be included to have a complete test of the converter prototype. Nonetheless, for first tests purposes, the laboratory power supply can also be used at lower power to assess if the port is functioning.

An extra 12 V rectifier is to be used to power up the driver boards of the bridges. For the control stage, the controller board will be initially fed directly by a USB connector to the PC host. An external supply could also be used, of either 3.3 V, 5 V or 7 to 12 V, depending on the configuration set at the board. It is however interesting to have the PC support at first so that phase shifts can be tuned easily without disconnecting the circuit.

6.2 Control Test

Once the prototype and sources are prepared, the testing process can start. Firstly, the control stage will be tested. The aim is to check if the control signals are well read by the driver boards of the bridges, and the gate signals of each MOSFETs correspond to the desired control. A little study on the deadtime introduction will also be done to set it correctly throughout the different bridges.

A small adjustment on the driver boards must be made to obtain the desired levels at the gates. Indeed, as it is shown in the schematics (included in the annex), some components are to be mounted . At the gate of both MOSFETs, a resistor is to be placed. A 20 Ω resistor is chosen for both gates and all boards, at recommendation. The value of the resistor can be tuned to have a faster rise and fall periods of the signal.

Moreover, a diode is needed for the bootstrap circuit. Its purpose is to sum up the high voltage gate signal with the output pin, as the V_{GS} signal is referenced to this middle point between the MOSFETs, rather than the ground as is the case for the low voltage side gate. It is consequently indispensable to run the HV gate to have this bootstrap circuit. A simple schottky diode is soldered in the board. After these small adjustments, the boards are ready to be tested. The same PicoScope tester as in the microcontroller programming stage will be used. The probes will be connected at each MOSFET gate to certify that the signal corresponds to its input control.

Once the functionality of the control stage is verified, an assessment on the configuration of the deadtime is to be done. Each half-bridge board introduces a configurable deadtime through a trimmer resistor (potentiometer). The voltage measurement through the trimmer is directly related to the introduced deadtime on the gate signals. It is important to mantain a safe margin to be sure not to cause a shortcircuit at any time between the two switches. Moreover, a too long deadtime may cause the converter not to correctly function, as the losses begin to increase due to the square signal being weaker and the effective period being reduced.

The trimmer has been firstly set so that the voltage signal at the deadtime pin is 2 V. Its resulting gate signals for both switches of the same board is shown in Figure 6.1. The observed deadtime between the fall of one signal and the rise of its complementary is 3 μs. This implies that, in a period of 10 μs, 60% of the time there is no output in any of the switches. It is therefore a too large number and it must be reduced.

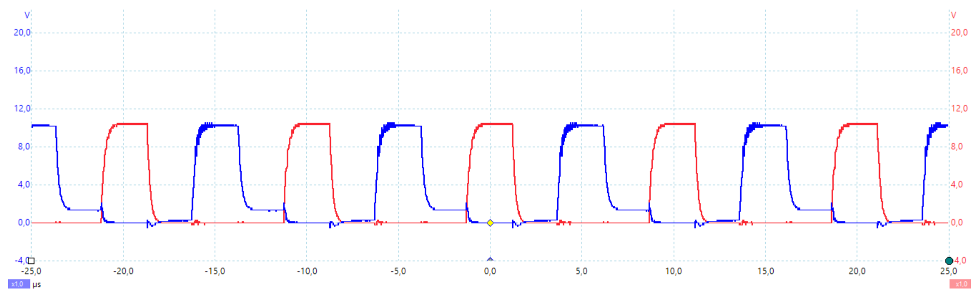

Figure 6.1: Gate signals of HV (blue) and LV(red) side with DT = 2 V.

It is also noticeable that the blue graph, which corresponds to the HV switch, has a small voltage value during the off time. This is due to the fact that the measurement has been taken in reference to the ground instead of the out signal, which is where the source of the MOSFET is connected. Even though there is no power side and therefore no voltage at the output, there is a small value that comes from the board simply being powered up. It is nonetheless negligible and not important for the test.

Figure 6.2 depicts the same two signals when the deadtime voltage level is 1 V. At first glance, it is visible that deadtime has been considerably reduced. Its value is now 2μs. It seems therefore that there is a direct correlation between the voltage level and the real deadtime: indeed, a reduction of 1 V has given a reduced deadtime by 1 μs. It is still a bit too high and it can be further improved. The voltage level of the signals is maintained at 10 V, sufficient for the MOSFET to activate.

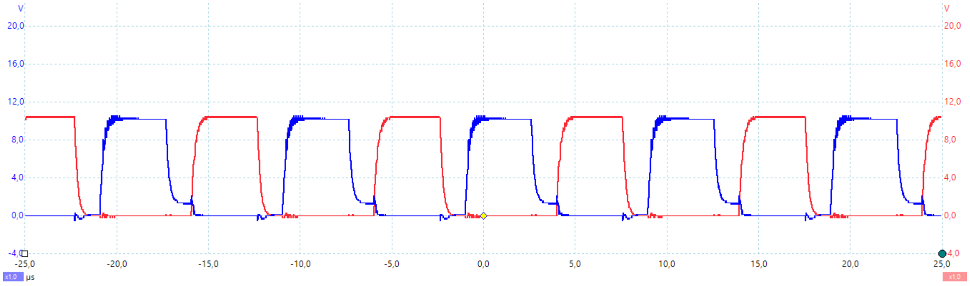

Figure 6.2: Gate signals of HV (blue) and LV(red) side with DT = 1 V.

Figure 6.3 shows the same signals with the deadtime configured at a voltage level of 0.35 V. At this level, the real deadtime is approximately of 1.35 μs, which validates the relation that was just established (it is difficult to asses with exactitude the deadtime as there is a bit of oscillations when the gate voltage changes its value). It is assumable that there is a 1 μs deadtime that is always present and cannot be avoided.

The latest value of deadtime, 0.35 V, will be taken as the established one for further tests. It has a good security margin while still maintaining the significance of the control signal and not loosing too much time and, consequently, power. All boards have been therefore set at the same level and the power tests are ready to start.

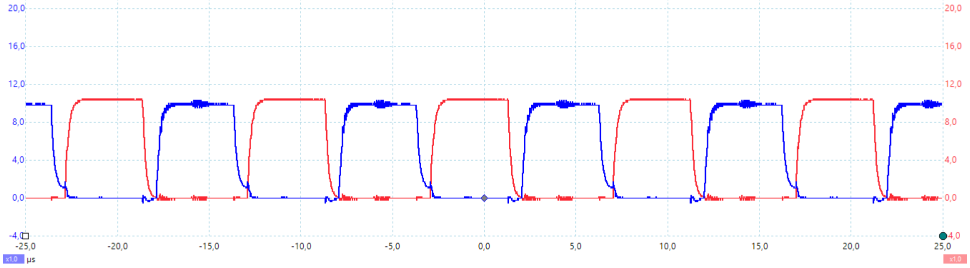

Figure 6.3: Gate signals of HV (blue) and LV(red) side with DT = 0.35 V.

6.3 Power Test

Once the bridges control has been successfully verified, the ports of the converter can be powered up to test its functionality. Firstly, a two-port test is to be performed to ease the verification analysis and successfully identify possible sources of errors and malfunctions.

Ports 1 and 2 will be firstly tested. The laboratory power source has been connected to port 1 and the load bank to port 2. The probes from the tester are connected to one of the output signals of each port, referenced to ground. The expected signal to be obtained is therefore a half positive square signal. Indeed, each half-bridge output accounts for half of the total square signal that were observed during simulation. As both outputs are complementary, it is enough to have the probe connected to one of them. It is also easier to assess switching oscillations and transients.

Indeed, on that note, when port 1 is supplied with 4 V, the graph in Figure 6.4 is obtained. As can be observed, there is a very large oscillation when the switching occurs. Even though the signal is established at a bit over 4 V, the spike gets to almost 20 V. This spike increases exponentially when trying to further increase the voltage, which makes it unsafe to do so.

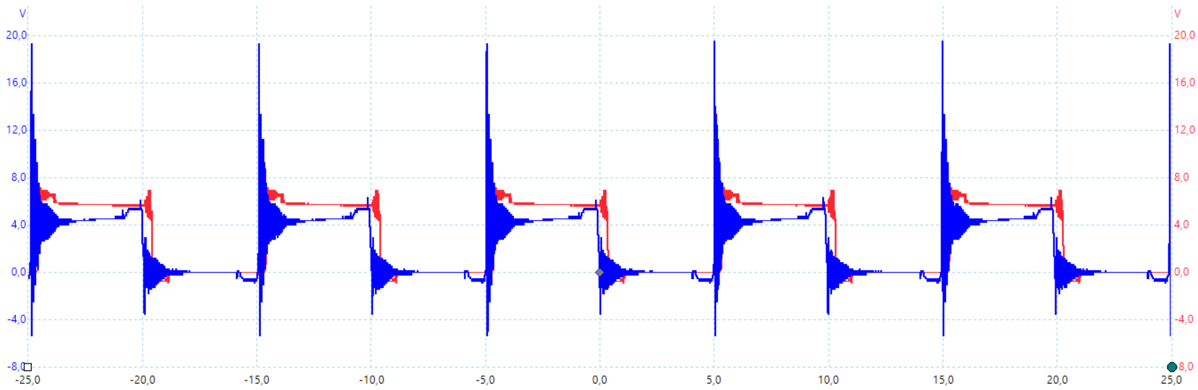

Figure 6.4: Output signals from a half-bridge of port 1 (blue) and port 2 (red).

Apart from the spike, the two square signals can be observed. The blue one corresponds to port 1, which is the supplying port, while the red graph corresponds to port 2, where the loads are connected. Both signals are phase-shifted 20 degrees for testing purposes. This shift can be observed in the graph. It is more clear in Figure 6.5, where the switching transient is shown in detail.

The observed oscillations are violent in dimension and rapid in time. The voltage level rises from zero to 20 V (5 times the final voltage level) in less than 60 ns. Oscillation continues in weaker form for about 1 μs, when the voltage is kept in a constant range. The repercussion of this oscillations and the way to avoid them will be explored after the performance of the first tests under low voltage.

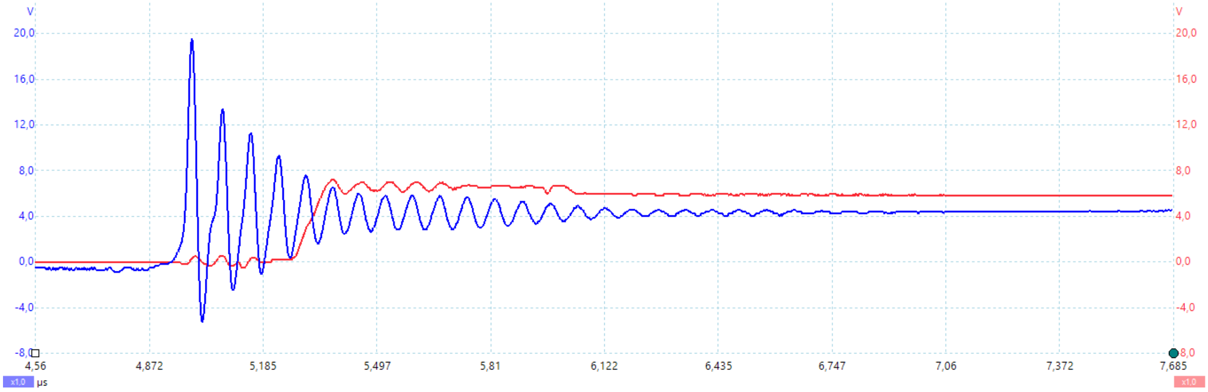

Figure 6.5: Detail of the switching transient of ports 1 (blue) and 2 (red).

As ports 1 and 2 are closely related when comparing their voltage level and turns ratio, it is preferable to involve port 3 (HV side) if a low power test is to be performed. Indeed, better result can extracted under these conditions if the load is connected to port 3 and the source is put on port 2.

After the connection of source and load, a test is performed at a low 5 V level. The resulting graphs are shown in Figure 6.6. The red graph depicts the output of a half-bridge of port 2, where the laboratory power supply is connected. Blue graph is the voltage output level of a half-bridge of port 3, where the loads are connected. The brown graph is the voltage at port 3, directly taken at the terminals of the load. A high voltage probe is in use, which divides by ten the resulting signal.

The supply is feeding the system at 5 V, with an input current of 0.57 A. The load output level is 1.8 V, with a 8.5 Ω resistance. As can be observed, input signal has the same violent spikes as observed before. Nonetheless, at this low power test, it can be seen that the output filter is indeed working, and feeding a constant voltage to the load at the same level as the square signal from the bridge output.

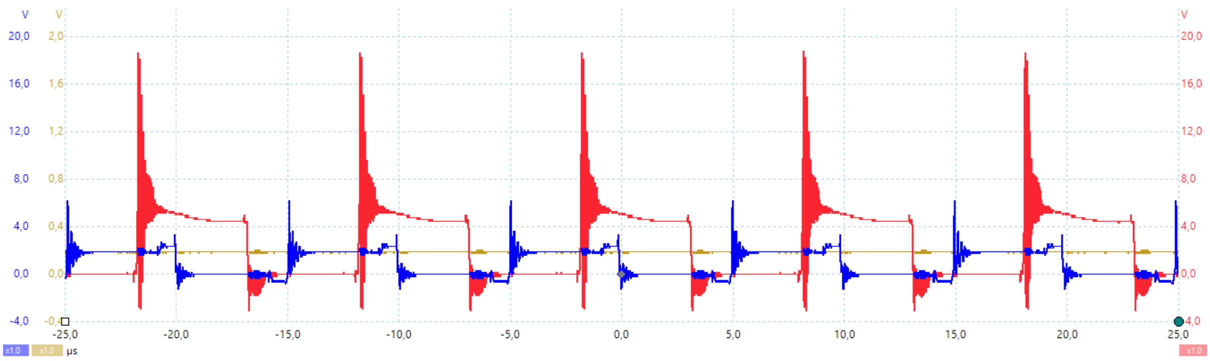

Figure 6.6: Output signal of a half-bridge of port 2 (red), port 3 (blue) and at load terminals (brown).

Figure 6.7 shows in detail both the output of the bridge in the load port and the corresponding voltage level at the terminals of the load. Even though the switching square signal also has some spikes when the switching occurs, the output signal is being well filtered and it is constant overall. This is a good sign of the converter functionality, as even in low power operation, the load port is showing the expected behaviour.

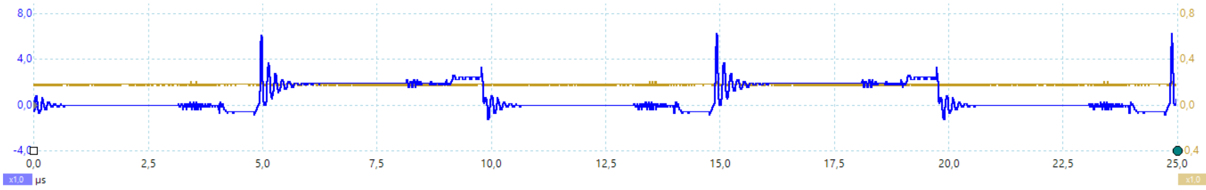

Figure 6.7: Output signal in port 3 (blue) and voltage at load terminals (brown).

As a higher-power test cannot be performed until the spike situation is solved, a further test will be performed with a load change. Indeed, the objective is to see if the output changes accordingly to a load increase. In the following situation, a second load of resistance 8.5Ω will be connected in parallel, converting the load in a resistance of 4.25 Ω. Figure 6.8 depicts this change, showing the same graphs as in the previous test.

While the input voltage (red graph) is maintained, the output voltage (blue and brown graphs) is changed accordingly to the load, with a reduction of half its voltage. The level is now down to 0.9 V, maintaining the 0.21 A of current through the load. It has therefore been proven that the output voltage is directly dependant of the connected load, as was to be expected according to simulations.

Furthermore, phase shift also plays a key role. During the test, phase shift 1-3 has been put at zero, as no power transfer occurs with port 1, while phase-shift 1-2 is set at -40 degree, representing the power transfer between ports 2 and 3. The values have been provisionally set just for testing purposes. If phase shift 1-2 were to be increased, the output would change accordingly as more power transfer would occur. Consequently, the output level depends directly on the load and the selected phase shift.

Figure 6.8: Output signal of port 2 (red), port 3 (blue) and at load terminals (brown) when load is double.

A detail of the obtained results is shown in Figure 6.9. The blue graph depicts the output of one of the half-bridges of the load port while the brown graph is the voltage level at the load terminals. The square signal in detail is similar to the previous test: indeed, spikes and transients follow the same pattern and are not influenced by the change in load. Spikes are still proportional in comparison with the load terminals voltage. As has been previously stated, the brown probe has a division factor of 10, which makes both graphs be at an equal value of 0.9 V.

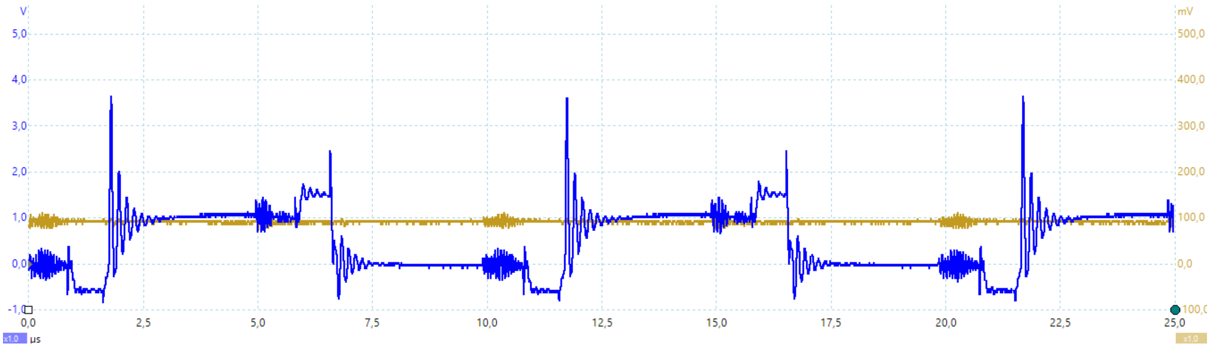

Figure 6.9: Output signal in port 3 (blue) and voltage at load (brown) when load is double.

To perform further tests at higher levels of power, the switching spikes problematic must be first solved. Indeed, as it is exponentially increasing, it would quickly get to voltage levels in which the components of the circuit could be in danger. A snubber has to be included in each bridge of the converter to deal with the transient voltage spikes.

A snubber is an electrical device aimed at suppresing the voltage transients occasioned by switching devices. As the connections throughout the bridges have some leakage inductance, it creates an inductive load which creates a sharp rise in voltage when the current supply is interrupted. The snubber creates an alternative circuit when put in parallel with the switching device, allowing for a safe discharge of the inductive load.

An RC type of snubber is to be used. It includes a small resistor in series with a capacitor which limits the voltage increase over time. Indeed, as a capacitor cannot have a sudden change of voltage in its terminals, a transient current will flow through it, allowing a more smoothly switching transition. As the resistance dissipates the charged energy, there is a small loss in efficiency throughout the system. Even though it can be a problem for commercial converters, it will not be of great issue for the prototype purpose.

For instance, when the MOSFET switch is off, the capacitor will charge through the resistance. When the switch is turned on, the opposite will occur, and the capacitor will be discharged through the resistor. This process will occur twice per switching period, as the snubber will be connected in parallel to the half-bridge. The snubber is also capable of modifying the ringing frequency, which can be interesting in case of electromagnetic interference.

To compute the necessary RC values two formulas can be used. First, regarding the capacitance, it can be put in relation with the peak current of the port and the voltage level over the rise time of the signal. Expressed in mathematical terms:

$$I_{peak} = C \cdot \frac{\Delta V}{\Delta t} \quad \rightarrow \quad C = I_{peak} \cdot \frac{\Delta t}{\Delta V} \tag{6.1}$$

To compute the resistance, the time constant of the RC snubber must be established. As a rule of thumb, a tenth of the switching time will be chosen. As there are two switching phases occuring per period, the formula is as follows:

$$\tau = R \cdot C \quad \rightarrow \quad R = \frac{\tau}{C} = \frac{1}{2 \cdot 10 \cdot f_{sw} \cdot C} \tag{6.2}$$

The snubber values can therefore be computed for all three ports. The rise time will be taken from the tests performed, which was 0.1 μs. Switching frequency is set at all bridges at 100 kHz. The voltage at each port is, as has been stated several times, 60 V, 48 V and 400 V, respectively for ports 1, 2 and 3. The peak currents, taken from the voltage range analysis, are 42 A, 55 A and 6 A, respectively. Computations are therefore as follows:

$$\begin{aligned} C_1 &= 42\ A \cdot \frac{0.1\ \mu s}{60\ V} = 70\ nF \\ R_1 &= \frac{1}{2 \cdot 10 \cdot 100\ kHz \cdot 70\ nF} = 7.143\ \Omega \end{aligned} \tag{6.3}$$

$$\begin{aligned} C_2 &= 55\ A \cdot \frac{0.1\ \mu s}{48\ V} = 114.58\ nF \\ R_2 &= \frac{1}{2 \cdot 10 \cdot 100\ kHz \cdot 114.58\ nF} = 4.364\ \Omega \end{aligned} \tag{6.4}$$

$$\begin{aligned} C_3 &= 6\ A \cdot \frac{0.1\ \mu s}{400\ V} = 1.5\ nF \\ R_3 &= \frac{1}{2 \cdot 10 \cdot 100\ kHz \cdot 1.5\ nF} = 333.33\ \Omega \end{aligned} \tag{6.5}$$

Computations were made so that, each cycle, the resistor is able to dissipate all the energy stored in the capacitor. The lost or dissipated power that would occur in the intended design can therefore be also computed:

$$P = E_c \cdot f_{sw} = 0.5 \cdot C \cdot V^2 \cdot f_{sw} \tag{6.6}$$

All computations are not included not to unnecessarily extend this procedure. All ports yield a dissipated power of around 12-13 W per half-bridge. To ease the soldering procedure and computations, the same snubber can be installed in each board. Indeed, the most dangerous spikes are coming from the low voltage side ports, as they have a higher current flowing. Therefore, the capacitance value will be taken at 100 nF, which is close enough to the computed value of both LV side ports.

As for the resistance, to reduce the consumption of power, a 1 Ω resistor can be taken. The rise time will consequently decrease. It is also advisable not to take a too large resistor as it could unnecessarily heat in excess. Nonetheless, if tests show that spikes are still too violent, its value can always be changed. The connection of the snubber to the full-bridge of each port is shown in Figure 6.10. The three ports would be in identical configuration.

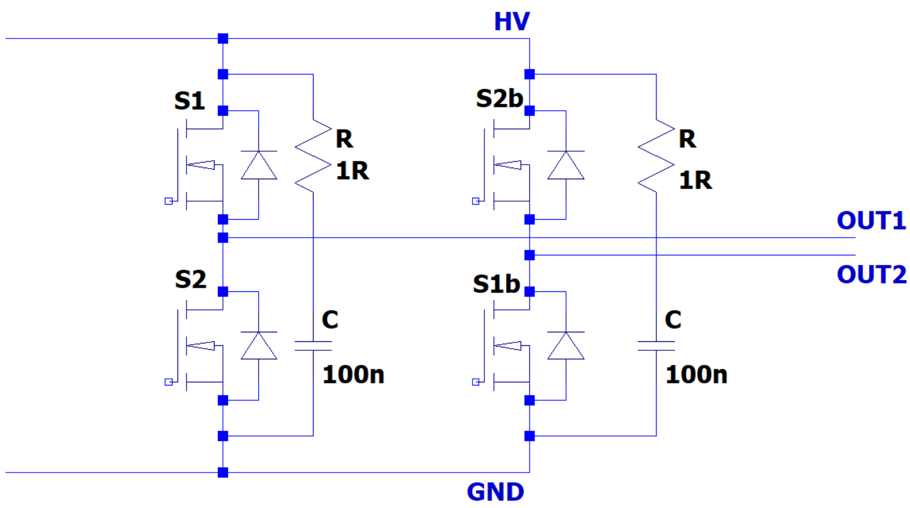

Figure 6.10: Snubber schematics when connected to one of the ports.

Further tests would include higher power once the snubber circuits were installed. First, the accuracy of the snubber should be attested, increasing progressively the power. Once the rated power has been successfully achieved, the different phase shift configurations and source/loads interactions would be tested, according to the three operating points established during waveform analysis. It would be necessary to assess the real phase shifts needed to achieve those situations and how do the waveforms compare to the simulation values, and in particular if ZVS conditions are still met.

Unfortunately, and due to timing constraints, further tests were not possible to be performed before the completion of this report. Nonetheless, work on the converter is to be continued further on, with the snubber installation as the next step and the mentioned tests as the short-term objective.

Chapter 7

Conclusions

The final chapter is dedicated to the conclusions drawn from the project that has been extensively developed throughout these pages. As different design aspects from the converter have been explored, different conclusions and verification have been obtained, and they can be classified in a similar manner as the project itself.

Firstly, several articles have been reviewed to explore the different topologies available for three-port bidirectional converters. Some configurations have been found to be of real interest, but only one has been chosen to be developed. The full-bridge topology, with the inclusion of two resonant tanks, presented a central power flow control that made it interesting for its simplicity and accessibility. Other aspects such as the possibility of lossless switching throughout its operating region made it appealing from an efficiency point of view.

The first set objective was to verify the theoretical formulas introduced in the reference paper. This has been done from two perspectives: theory itself, with an analysis of the formulas, and from simulation of the converter, assessing its functionality and trying to obtain the same parameters as those obtained using the mentioned formulas. This verification has been successful, as both simulation and theory have yielded the same values of current transfer and phase shift at the analyzed operating points.

Moving forward from it, the reference paper has been left behind and new parameters have been set to design a converter that could meet the required criteria for the purpose at hand. Again, theoretical computations and simulation have been done under these new parameters to assess if the converter still worked in a similar manner and to check what was to be expected from it. The conclusions were once again satisfactory, as it was found that both theory and simulation yielded the same current and phase shift result overall.

A prototype of the converter has been built aiming at performing an experimental validation of it. The different components that formed up the prototype have been accordingly justified. A special focus has been put on the magnetics design, as the three-winding transformer and the two resonant inductors have been manually built in the laboratory. The preliminary tests on the designed magnetic components yielded satisfactory results, and the prototype was validated. A further exploration on the control part has also been performed, with special emphasis on the modes available to generate the different control signal and their interaction among each other.

Finally, a testing phase has been done on the built prototype. First, control test has yielded a satisfactory result on the driver boards after some modifications were made. Power tests rose some technical difficulties regarding undesired spikes in voltage signal during switching. They were explored and their nature justified. Furthermore, the filtering solution has been designed to be able to do further power tests. Preliminary tests gave satisfactory output results on the connected load, but further progress could not be made at the end of this project report due to time constraints. Progress is set to continue in the following days to complete the testing process and, consequently, the experimental validation of the converter.

7.1 Future Work

Once the converter design is validated, there is considerable room for improvement in its capabilities. Future work on the prototype would be required to be able to have a commercially ready solution to be installed in SBIPV systems.

The implemented control required the phase shifts to be manually introduced in the programming of the microcontroller. A closed-loop design would allow the converter to manually set itself to the required operating point measuring just two parameters of the system, such as the output voltage and the current injected from port 1. Furthermore, different modes could be programmed to allow the end user to select its preferred configuration. For instance, one could prefer to have the distribution side be always fed by the PV panels when there is energy available. An energy management system could allow interaction with the energy market and switch the consumption to the battery whenever prices are higher, or even sell energy if an interconnection of the system is done.

Regarding the hardware side, the prototype should be perfected and improved. A PCB could be laid out to connect all the different components in a more compact way. A module could be designed to be installed around the converter and be integrated into larger scale cabinets and other electrical systems. Different filtering designs could be explored to improve both the efficiency and the energy density of the converter. In conclusion, future work would involve a more compact and efficient converter that could satisfy the requirements of every user and be easily installed in newly designed buildings with SBIPV systems.

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Appendix A

Strategic Aspects of CE+T Energrid

CE+T (Constructions Électroniques + Télécommunications) was founded in 1934. It has been specialized in the power electronics field since the 1960s. At the end of the 1980s, the company invented a modular inverter that lead them to be on top of the international market, with power solutions like the mentioned inverters, but also modular UPS and other ranges of products that were added through the years.

In 2017, a spin-out company was founded: CE+T Energrid. It is still working under close collaboration with their mother company, CE+T Power, with which they share part of their sales and technical teams. The operational team fully integrated in the Energrid division is composed of 4 members, including both software and hardware engineers, a project manager and a business development manager. They have over 2 million euros in funding and expect to keep increasing their size in the coming years.

They center their business on three different needs around the energy management domain. Firstly, the need for portable energy for different types of applications; secondly, the need for energy conditioning, such as filtering of power disturbances or backup solutions; and lastly, energy storage solutions for all types of customers: residential, commercial or industrial.

On the portable energy domain, CE+T Energrid bases its technology on their achievement in 2016, when they won the Little Box Challenge contest organized by Google. The contest consisted in designing the smallest power converter in the world, with a minimum power density of 50 $^{W}/_{in^3}$. The solution created by CE+T had a power density of 145.24 $^{W}/_{in^3}$, which made them win the grand prize of 1 million dollars. The company CE+T Energrid was created to develop this successful technology and be able to sell it on the market.

The energy conditioning solutions are focused on reducing at maximum the energy bill of the customer. Batteries are used to store energy and reduce peak consumption; an energy management system is used to transfer energy in 3-phase system to balance the difference phases; and power conversion and storage systems are used to filter all disturbances from the network. Reliability and cost reducing are key elements of the products offered by the company. Moreover, their modular approach allows the customer to invest little by little in the products, which makes it an attractive solution for middle customers that could not afford the whole investment cost.

Energy storage solutions are essential nowadays with the rise of renewable energies, in which production time does not meet consumption. Microgrids are therefore becoming more and more popular nowadays. In them, one or several customers share an electrical system, consisting of generation, storage and consumption stages. All is interconnected through power converters and managed with energy management system software. It allows the users to reduce their energy bill, even being able to sell their excess of energy to the electricity market. It also has more uses such as backup power systems or charging stations for electrical vehicles.

The first microgrid project developed by the company is called Merygrid. The development of the project, in close collaboration with the University of Liège, is aimed at being a proof of concept. It interconnects three different companies located close together in the same region. The source of power comes from both a photovoltaic system and hydropower. The microgrid must be able to effectively cover the consumption of the three companies with the aid of a battery system as well as the required power converters, developed by the company. The energy management system, developed by the University of Liège, allows for data interface and management as well as real time and predictive control.

For residential customers, energy storage solutions are also being developed by the company. They work in close collaborations with other companies which provide the battery and inverter modules. The battery management system is of key importance to harvest at maximum the benefits of these systems for particular customers who do not have great needs but wish to have their electrical bill reduced. It is therefore important to keep the investment from the user worthy in the minimum span of time possible.

CE+T Energrid is fixed by some strong values that they try to reproduce in every aspect of their work. For instance, their green responsibility does not only involve the color of their logo. All products from the company are optimized to have the highest power factor possible, being able to convert more power in less space. Improving the efficiency allows to use at maximum the power that is being generated and reduces significantly its losses. Moreover, they use either recycled or recyclable materials in all their packaging methods.

The factories of the CE+T group are powered by renewable energies, by means of mainly photovoltaic systems. This reduces the footprint of the company at minimum and allows them to be proud of their environmental responsibility. Not only they focus their business in renewable solutions that allow to reduce CO2 emissions, but they also lead the example by generating the power that they consume in a clean way.

CE+T is present all around the world, with sites in China, India, Luxembourg and the USA among others, along with Belgium where their headquarters are based. Besides the technology divisions, they have sales teams working all around the globe for the international markets, where they try to position their products according to the specific needs of the region. The company and the group itself is in continuous expansion, not only growing into new markets but also increasing their presence in already explored markets.

Their selling approach is the reliability and quality of their products. Indeed, customers seeking CE+T usually require solutions that are technologically at the top of the competition and allow them to improve their respective businesses further on. Every unit of power counts, and every second without power produces high losses for the group's customers. CE+T proudly introduces their products as the most reliable on the market, and their many technological inventions support the claim. Investment in R&D is therefore one of the key aspects of the group, with new products always on development.

The group and, in particular, the Energrid division, is always present in the most important events from the energy management domain. All around the globe, they have participated in countless workshops and conferences. As they have experts from many different nationalities, they are able to present their products with a sales representative from that market that creates a closer bound with the customers attending the event in their home country. Proximity is one of the key roles in the sales department strategy, while maintaining their international approach.

Over 80 years of history have shaped CE+T as one of the leading groups in the power electronics domain. They have been able to shift their focus and product range at each era, maintaining themselves on the top of the market. Their technological innovation is what defines the group, and specially Energrid which was born from an award-winning invention. Customers associate the brand with reliability, pioneering technology and proximity. These strong values are the most valuable asset of CE+T and they are what define them as one of the strongest competitors on the market.

Appendix B

Bill of Materials

Designator	Qty	Part Number	Manufacturer	Description
MC	1	NUCLEO-F207ZG	ST	Control Dev Board
P1A, P1B, P2A, P2B, P3A, P3B	6	EVAL6494L	ST	Driver Dev Board
S1, S1b, S2, S2b	8	IRFP4321PBF	Infineon	MOSFET, N-CH, 150V, 78A, 15,5mohm
S5, S6	4	STW28N65M2	ST	MOSFET, N-CH, 650V, 20A, 180mohm
C1	10	C1210C223-KBGACTU	KEMET	CAP, CERM, 22nF, 630V, C0G
C1	1	C3225NP02J-103J125AA	TDK	CAP, CERM, 10nF, 630V, C0G
C2	10	C3225C0G2-J153J160AE	TDK	CAP, CERM, 15 nF, 630V, C0G
Cf2	1	B32778P7306K000	TDK	CAP, AL, 30μF, 700V, 18,5A
Cf3	1	C4AQQB-W5120A3FJ	KEMET	CAP, AL, 12μF, 1100V, 10A
TFO	2	ETD49/25/16-3C95	FERROXCUBE	Transformer Core
L1, L2	4	E55/28/25-3C95	FERROXCUBE	Inductor Core
TFO	4m	LW160*AWG42	PACK Feindrähte	LitzWire 160 AWG 42
L1,L2,TFO	5m	LW630*AWG41	PACK Feindrähte	LitzWire 630 AWG 41
-	3	RE200-LF	ROTH	Prototyping Eurocard Board
-	2	BCS117-L-D-TE	Samtec Inc.	Connector 34 contacts

Table B.1: Bill of Materials of the converter.

Appendix C

Component Ratings

The following table enumerates all components included in the converter with their description, their value (if applicable), and the maximum ratings of voltage and current (both rms and peak values) that they have to withstand, according to the operation and voltage range analysis of the converter.

Comp.	**Description**	**Value**	I_{rms} **(A)**	I_{peak} **(A)**	V_{rms} **(V)**	V_{peak} **(V)**
C1	Cap Tank 1	0.15 μF	30.00	42.00	320.00	450.00
C2	Cap Tank 2	0.23 μF	40.00	55.00	278.00	393.00
L1	Ind Tank 1	20.43 μH	30.00	42.00	388.00	560.00
L2	Ind Tank 2	13.08 μH	40.00	55.00	333.00	480.00
Cf2	Cap filter 2	32.00 μF	14.15	37.50	48.00	48.00
Cfo	Cap filter 3	12.00 μF	4.75	8.50	400.00	400.00
S1.1	MOSFET P1A.1	-	21.34	42.00	42.23	60.00
S1.2	MOSFET P1A.2	-	21.34	42.00	42.23	60.00
S1.3	MOSFET P1B.1	-	21.34	42.00	42.23	60.00
S1.4	MOSFET P1B.2	-	21.34	42.00	42.23	60.00
S2.1	MOSFET P2A.1	-	28.24	55.00	34.44	48.00
S2.2	MOSFET P2A.2	-	28.24	55.00	34.44	48.00
S2.3	MOSFET P2B.1	-	28.24	55.00	34.44	48.00
S2.4	MOSFET P2B.2	-	28.24	55.00	34.44	48.00
S3.1	MOSFET P3A.1	-	1.87	6.00	287.22	400.00
S3.2	MOSFET P3A.2	-	1.87	6.00	287.22	400.00
S3.3	MOSFET P3B.1	-	1.87	6.00	287.22	400.00
S3.4	MOSFET P3B.2	-	1.87	6.00	287.22	400.00
Lp1	Port 1 winding	0.15	30.00	42.00	60.00	60.00
Lp2	Port 2 winding	0.12	40.00	55.00	48.00	48.00
Ls	Port 3 winding	1.00	4.75	8.50	400.00	400.00

Table C.1: Component ratings of the converter.

Appendix D

Schematics

Four different schematics are included in this annex. The first three correspond to the converter itself and have been personally developed with the QElectroTech software. The fourth one corresponds to the half-bridge driver boards and is included in their datasheet.

First schematics, entitled 'Ports view', envisions the converter prototype from a theoretical point of view, that is, separating all the components into their respective ports. It does not correspond to the actual configuration of the prototype but it rather serves as a transition between the circuit schematics depicted during theoretical computations and the translation of each part to its real component.

Second schematic is entitled 'Block view'. It is a closely related image from the final prototype. It distinguishes the converter between the Power stage, the microcontroller and the different sources. It is a view that allows the reader to understand the different parts in which the converter is divided.

Third schematics is entitled 'Connexion view'. In this schematic, no connection tags are used but rather all connections are explicitly drawn, as the aim is to get as close as possible to the prototype configuration. It could also be refered as the prototype assembly schematic, as it reflects all the connections that must be put in the prototype to connect every part of the converter. Signals are closely connected to their respective grounds to reduce noise as was envisioned during the prototype assembly section.

Lastly, the fourth included schematics corresponds to the half-bridge development board. It is included in the datasheet of the mentioned board. It shows all pin connections and how they interact with each other, as well as the components missing and to be mounted (both MOSFETs, resistances in the gate signals side and a diode for the bootstrap capability). It is consequently of special interest as a lot of extra work has been done unto the board and some components have been added, as explained during the corresponding prototyping section.

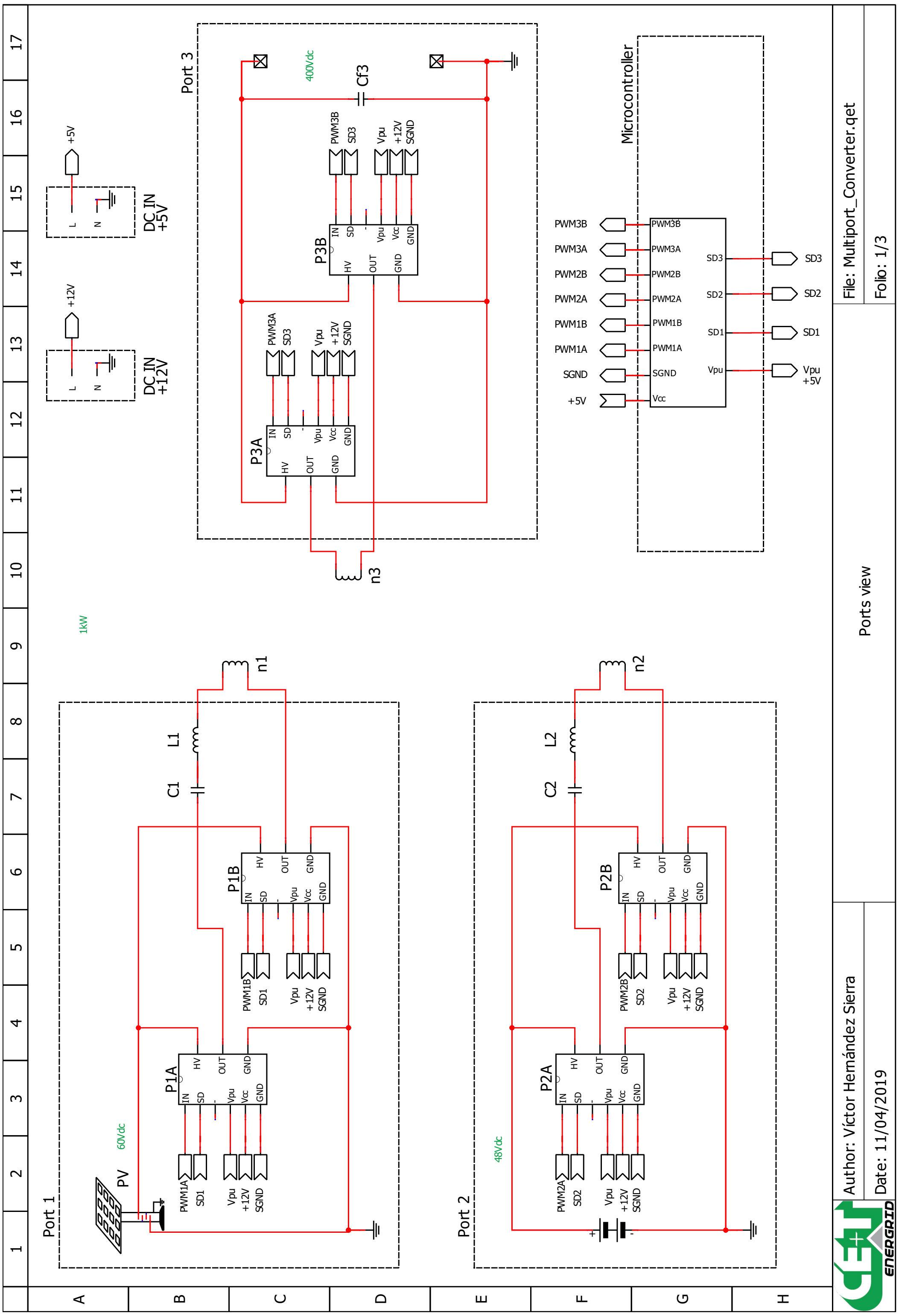

Figure D.1: Ports view schematic of the converter.

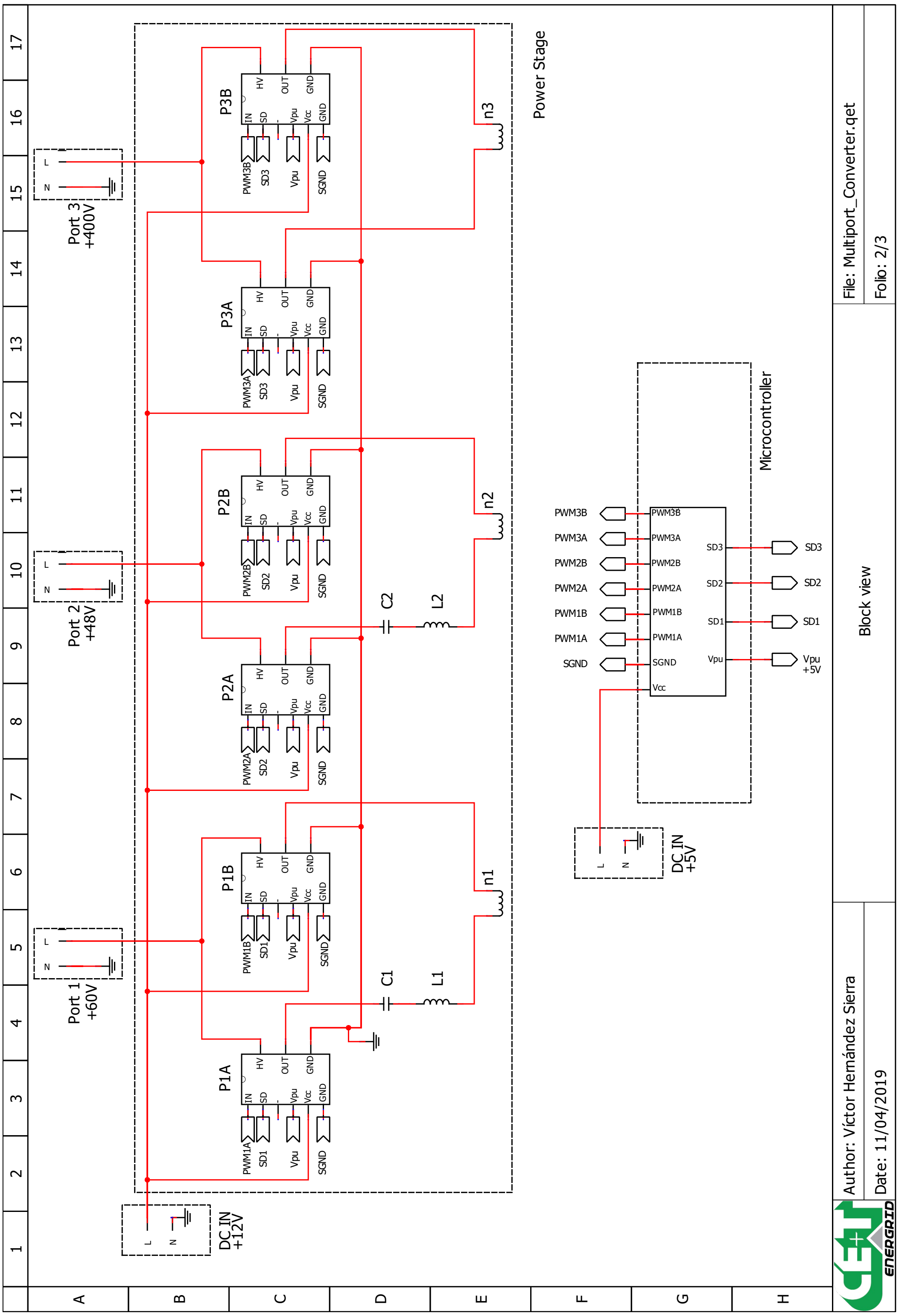

Figure D.2: Block view schematic of the converter.

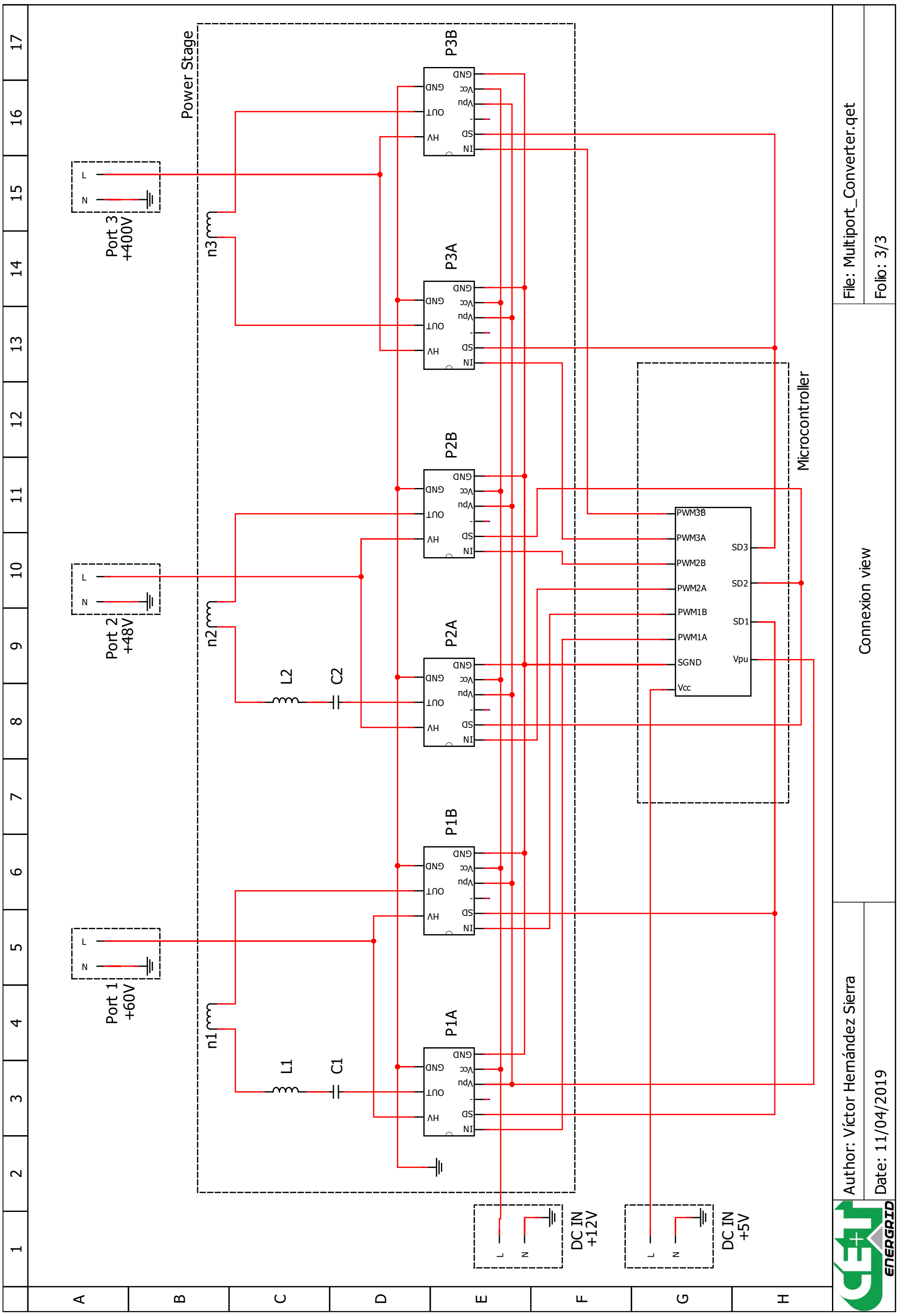

Figure D.3: Connexion view schematic of the converter.

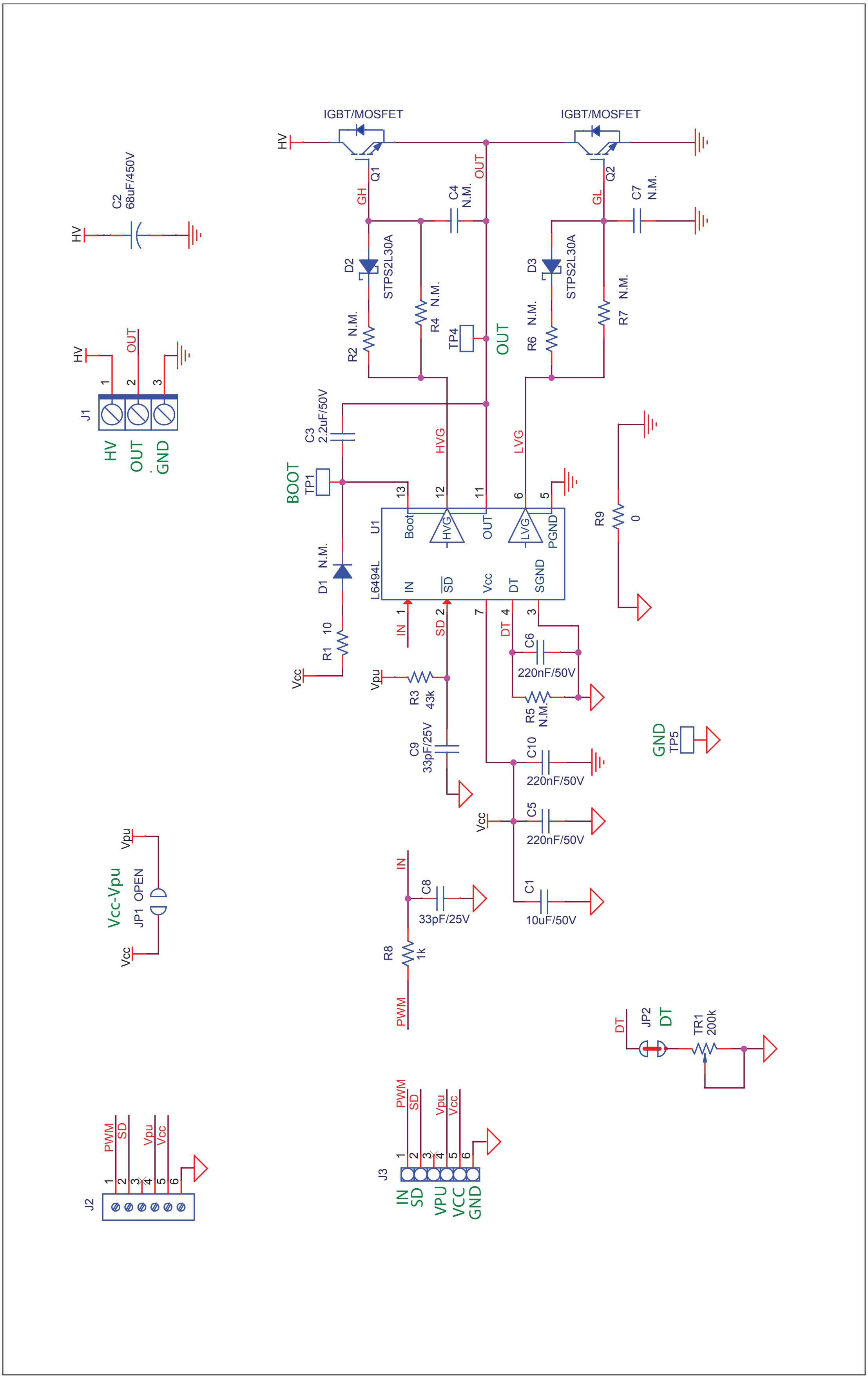

Figure D.4: Half-Bridge Driver Devlopment Board Schematics.

Appendix E

Microcontroller Code

```
/* Includes                                          */
#include "main.h"

/* Private variables                                 */
ETH_HandleTypeDef heth;
TIM_HandleTypeDef htim1;
UART_HandleTypeDef huart3;
PCD_HandleTypeDef hpcd_USB_OTG_FS;
int degree2;
int degree3;
int pulse1;
int pulse2;
int pulse3;

/* Private function prototypes                       */
void SystemClock_Config(void);
static void MX_GPIO_Init(void);
static void MX_ETH_Init(void);
static void MX_TIM1_Init(void);
static void MX_USART3_UART_Init(void);
static void MX_USB_OTG_FS_PCD_Init(void);

/**
  * @brief  The application entry point.
  * @retval int
  */
int main(void)
{
  /* degree2 and degree3 to be set (phase shifts 1 2 and 1 3) */
  degree2 = 0;
  degree3 = 0;
  /* Pulse value to be set at CCR registry according to phase shift */
  pulse1 = 1;
  pulse2 = degree2*600/180;
  pulse3 = degree3*600/180;
  /* Special cases of phase shift values */
  if (degree2 <= 0 || degree2 > 90) {
    pulse2 = 1;
  }
  if (degree3 < 90 || degree3 == 0 || degree3 >= 180) {
    pulse3 = 1;
  }
```

```
  if ( 90 >= degree3 < 0) {
    pulse1 =  pulse3;
    pulse2 = pulse2    pulse3;
    pulse3 = 1;
  }

  /* MCU Configuration
                                                                        */
  /* Reset all peripherals, Initializes Flash interface and Systick. */
  HAL_Init();
  /* Configure the system clock */
  SystemClock_Config();
  /* Initialize all configured peripherals */
  MX_GPIO_Init();
  MX_ETH_Init();
  MX_TIM1_Init();
  MX_USART3_UART_Init();
  MX_USB_OTG_FS_PCD_Init();
  /* Outputs initialization (code not generated by software) */
  HAL_TIM_OC_Start(&htim1, TIM_CHANNEL_1);
  HAL_TIMEx_OCN_Start(&htim1, TIM_CHANNEL_1);
  HAL_TIM_OC_Start(&htim1, TIM_CHANNEL_2);
  HAL_TIMEx_OCN_Start(&htim1, TIM_CHANNEL_2);
  HAL_TIM_OC_Start(&htim1, TIM_CHANNEL_3);
  HAL_TIMEx_OCN_Start(&htim1, TIM_CHANNEL_3);
  /* Infinite loop */
  while (1)
  {
  }
}

/**
  * @brief System Clock Configuration
  * @retval None
  */
void SystemClock_Config(void)
{
  RCC_OscInitTypeDef RCC_OscInitStruct = {0};
  RCC_ClkInitTypeDef RCC_ClkInitStruct = {0};
  /** Initializes the CPU, AHB and APB busses clocks */
  RCC_OscInitStruct.OscillatorType = RCC_OSCILLATORTYPE_HSI;
  RCC_OscInitStruct.HSIState = RCC_HSI_ON;
  RCC_OscInitStruct.HSICalibrationValue = RCC_HSICALIBRATION_DEFAULT;
  RCC_OscInitStruct.PLL.PLLState = RCC_PLL_ON;
  RCC_OscInitStruct.PLL.PLLSource = RCC_PLLSOURCE_HSI;
  RCC_OscInitStruct.PLL.PLLM = 13;
  RCC_OscInitStruct.PLL.PLLN = 195;
  RCC_OscInitStruct.PLL.PLLP = RCC_PLLP_DIV2;
  RCC_OscInitStruct.PLL.PLLQ = 5;
  if (HAL_RCC_OscConfig(&RCC_OscInitStruct) != HAL_OK)
  {
    Error_Handler();
  }
  /** Initializes the CPU, AHB and APB busses clocks */
  RCC_ClkInitStruct.ClockType = RCC_CLOCKTYPE_HCLK|RCC_CLOCKTYPE_SYSCLK
                              |RCC_CLOCKTYPE_PCLK1|RCC_CLOCKTYPE_PCLK2;
  RCC_ClkInitStruct.SYSCLKSource = RCC_SYSCLKSOURCE_PLLCLK;
  RCC_ClkInitStruct.AHBCLKDivider = RCC_SYSCLK_DIV1;
```

```
  RCC_ClkInitStruct.APB1CLKDivider = RCC_HCLK_DIV4;
  RCC_ClkInitStruct.APB2CLKDivider = RCC_HCLK_DIV2;
  if (HAL_RCC_ClockConfig(&RCC_ClkInitStruct, FLASH_LATENCY_3) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief ETH Initialization Function
  * @param None
  * @retval None
  */
static void MX_ETH_Init(void)
{
  uint8_t MACAddr[6] ;
  heth.Instance = ETH;
  heth.Init.AutoNegotiation = ETH_AUTONEGOTIATION_ENABLE;
  heth.Init.PhyAddress = LAN8742A_PHY_ADDRESS;
  MACAddr[0] = 0x00;
  MACAddr[1] = 0x80;
  MACAddr[2] = 0xE1;
  MACAddr[3] = 0x00;
  MACAddr[4] = 0x00;
  MACAddr[5] = 0x00;
  heth.Init.MACAddr = &MACAddr[0];
  heth.Init.RxMode = ETH_RXPOLLING_MODE;
  heth.Init.ChecksumMode = ETH_CHECKSUM_BY_HARDWARE;
  heth.Init.MediaInterface = ETH_MEDIA_INTERFACE_RMII;
  if (HAL_ETH_Init(&heth) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief TIM1 Initialization Function
  * @param None
  * @retval None
  */
static void MX_TIM1_Init(void)
{
  TIM_ClockConfigTypeDef sClockSourceConfig = {0};
  TIM_MasterConfigTypeDef sMasterConfig = {0};
  TIM_OC_InitTypeDef sConfigOC = {0};
  TIM_BreakDeadTimeConfigTypeDef sBreakDeadTimeConfig = {0};
  htim1.Instance = TIM1;
  htim1.Init.Prescaler = 0;
  htim1.Init.CounterMode = TIM_COUNTERMODE_UP;
  htim1.Init.Period = 599;
  htim1.Init.ClockDivision = TIM_CLOCKDIVISION_DIV1;
  htim1.Init.RepetitionCounter = 0;
  htim1.Init.AutoReloadPreload = TIM_AUTORELOAD_PRELOAD_DISABLE;
  if (HAL_TIM_Base_Init(&htim1) != HAL_OK)
  {
    Error_Handler();
  }
  sClockSourceConfig.ClockSource = TIM_CLOCKSOURCE_INTERNAL;
```

```
  if (HAL_TIM_ConfigClockSource(&htim1, &sClockSourceConfig) != HAL_OK)
  {
    Error_Handler();
  }
  if (HAL_TIM_OC_Init(&htim1) != HAL_OK)
  {
    Error_Handler();
  }
  sMasterConfig.MasterOutputTrigger = TIM_TRGO_RESET;
  sMasterConfig.MasterSlaveMode = TIM_MASTERSLAVEMODE_DISABLE;
  if (HAL_TIMEx_MasterConfigSynchronization(&htim1, &sMasterConfig) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.OCMode = TIM_OCMODE_TOGGLE;
  sConfigOC.Pulse = pulse1;
  sConfigOC.OCPolarity = TIM_OCPOLARITY_HIGH;
  sConfigOC.OCNPolarity = TIM_OCNPOLARITY_HIGH;
  sConfigOC.OCFastMode = TIM_OCFAST_DISABLE;
  sConfigOC.OCIdleState = TIM_OCIDLESTATE_RESET;
  sConfigOC.OCNIdleState = TIM_OCNIDLESTATE_RESET;
  if (HAL_TIM_OC_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_1) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.Pulse = pulse2;
  sConfigOC.OCIdleState = TIM_OCIDLESTATE_SET;
  if (HAL_TIM_OC_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_2) != HAL_OK)
  {
    Error_Handler();
  }
  sConfigOC.Pulse = pulse3;
  if (HAL_TIM_OC_ConfigChannel(&htim1, &sConfigOC, TIM_CHANNEL_3) != HAL_OK)
  {
    Error_Handler();
  }
  sBreakDeadTimeConfig.OffStateRunMode = TIM_OSSR_DISABLE;
  sBreakDeadTimeConfig.OffStateIDLEMode = TIM_OSSI_DISABLE;
  sBreakDeadTimeConfig.LockLevel = TIM_LOCKLEVEL_OFF;
  sBreakDeadTimeConfig.DeadTime = 0;
  sBreakDeadTimeConfig.BreakState = TIM_BREAK_DISABLE;
  sBreakDeadTimeConfig.BreakPolarity = TIM_BREAKPOLARITY_HIGH;
  sBreakDeadTimeConfig.AutomaticOutput = TIM_AUTOMATICOUTPUT_DISABLE;
  if (HAL_TIMEx_ConfigBreakDeadTime(&htim1, &sBreakDeadTimeConfig) != HAL_OK)
  {
    Error_Handler();
  }
  HAL_TIM_MspPostInit(&htim1);
}

/**
  * @brief USART3 Initialization Function
  * @param None
```

```
  * @retval None
  */
static void MX_USART3_UART_Init(void)
{
  huart3.Instance = USART3;
  huart3.Init.BaudRate = 115200;
  huart3.Init.WordLength = UART_WORDLENGTH_8B;
  huart3.Init.StopBits = UART_STOPBITS_1;
  huart3.Init.Parity = UART_PARITY_NONE;
  huart3.Init.Mode = UART_MODE_TX_RX;
  huart3.Init.HwFlowCtl = UART_HWCONTROL_NONE;
  huart3.Init.OverSampling = UART_OVERSAMPLING_16;
  if (HAL_UART_Init(&huart3) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief USB_OTG_FS Initialization Function
  * @param None
  * @retval None
  */
static void MX_USB_OTG_FS_PCD_Init(void)
{
  hpcd_USB_OTG_FS.Instance = USB_OTG_FS;
  hpcd_USB_OTG_FS.Init.dev_endpoints = 4;
  hpcd_USB_OTG_FS.Init.speed = PCD_SPEED_FULL;
  hpcd_USB_OTG_FS.Init.dma_enable = DISABLE;
  hpcd_USB_OTG_FS.Init.phy_itface = PCD_PHY_EMBEDDED;
  hpcd_USB_OTG_FS.Init.Sof_enable = ENABLE;
  hpcd_USB_OTG_FS.Init.low_power_enable = DISABLE;
  hpcd_USB_OTG_FS.Init.vbus_sensing_enable = ENABLE;
  hpcd_USB_OTG_FS.Init.use_dedicated_ep1 = DISABLE;
  if (HAL_PCD_Init(&hpcd_USB_OTG_FS) != HAL_OK)
  {
    Error_Handler();
  }
}

/**
  * @brief GPIO Initialization Function
  * @param None
  * @retval None
  */
static void MX_GPIO_Init(void)
{
  GPIO_InitTypeDef GPIO_InitStruct = {0};
  /* GPIO Ports Clock Enable */
  __HAL_RCC_GPIOC_CLK_ENABLE();
  __HAL_RCC_GPIOH_CLK_ENABLE();
  __HAL_RCC_GPIOA_CLK_ENABLE();
  __HAL_RCC_GPIOE_CLK_ENABLE();
  __HAL_RCC_GPIOB_CLK_ENABLE();
  __HAL_RCC_GPIOD_CLK_ENABLE();
  __HAL_RCC_GPIOG_CLK_ENABLE();
  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(GPIOB, LD3_Pin|LD2_Pin, GPIO_PIN_RESET);
```

```
  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(USB_PowerSwitchOn_GPIO_Port, USB_PowerSwitchOn_Pin,
    GPIO_PIN_RESET);
  /*Configure GPIO pin Output Level */
  HAL_GPIO_WritePin(LD1_GPIO_Port, LD1_Pin, GPIO_PIN_RESET);
  /*Configure GPIO pin : USER_Btn_Pin */
  GPIO_InitStruct.Pin = USER_Btn_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_IT_RISING;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  HAL_GPIO_Init(USER_Btn_GPIO_Port, &GPIO_InitStruct);
  /*Configure GPIO pins : LD3_Pin LD2_Pin */
  GPIO_InitStruct.Pin = LD3_Pin|LD2_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
  HAL_GPIO_Init(GPIOB, &GPIO_InitStruct);
  /*Configure GPIO pin : USB_PowerSwitchOn_Pin */
  GPIO_InitStruct.Pin = USB_PowerSwitchOn_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
  HAL_GPIO_Init(USB_PowerSwitchOn_GPIO_Port, &GPIO_InitStruct);
  /*Configure GPIO pin : USB_OverCurrent_Pin */
  GPIO_InitStruct.Pin = USB_OverCurrent_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_INPUT;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  HAL_GPIO_Init(USB_OverCurrent_GPIO_Port, &GPIO_InitStruct);
  /*Configure GPIO pin : LD1_Pin */
  GPIO_InitStruct.Pin = LD1_Pin;
  GPIO_InitStruct.Mode = GPIO_MODE_OUTPUT_PP;
  GPIO_InitStruct.Pull = GPIO_NOPULL;
  GPIO_InitStruct.Speed = GPIO_SPEED_FREQ_LOW;
  HAL_GPIO_Init(LD1_GPIO_Port, &GPIO_InitStruct);
}
/*****END OF FILE****/
```