Master's Thesis : Simulation of a programmable RLC impedance (analog and digital implementation)

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Simulation of a programmable RLC impedance

Analog and digital implementation

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Abstract

Different kinds of electronic load simulators for testing of power supply have been developed and commercialised. A programmable RLC impedance with adjustable R, L and C can be useful to simulate the load of a generator like a motor for example. Some companies may be interested in testing their voltage/current generators under some conditions and study their behaviours. Both inductive and capacitive loads can be simulated by adjusting the phase difference between the voltage and current waveforms. However, there exist many drawbacks, for example, it can provide only 4 modes including constant resistance (pure resistive load), constant power, constant current and constant voltage to simulate simple dc loads. But more often, they cannot simulate a RL or RC load with a good dynamic response. The main objective of this master thesis is to design, manufacture and test a programmable RLC impedance. This circuit must cover the entire inductive-resistive-capacitive range (voltage/current phase shift between $-90°$ and $90°$). The RLC load must be able to dissipate up to 5 W. Two different implementations are suggested : the analog and digital RLC impedance with their pros and cons.

The first step is to design an analog impedance. A gyrator is used in order to simulate a non ideal inductor with parallel redundant resistor. The main property of the gyrator is to invert the current-voltage characteristic of an electrical component. This way, a capacitor can be used to get a non ideal variable inductor. The inductance can be adjusted with simple potentiometers. The second step consists in removing the parallel resistors in order to simulate an ideal inductor and reach the $90°$ phase-shift. This objective can be achieved by connecting the Negative Impedance Converter (N.I.C) in parallel to the gyrator. After that, a more detailed study of the output current and output voltage across the op amps allows to highlight the main limitations of such circuits. The voltage and current saturation of the op amps limit the available range of inductance/capacitance values. Several simulations with a real precision op amp (AD744) are performed. Finally, those circuits have been implemented on a breadboard in the CSL laboratory[1] with commercial op amps such as the famous LM324. The

[1]For more information about the CSL, see Appendix C.

results in terms of output current are compared with the simulations.

The second step consists in designing a digital RLC impedance. By contrast to the analog impedance, the filtering process is done digitally using the microcontroller ATMEGA2560. A software feedback control approach is employed to adjust the current amplitude and the power factor. The objective is to maintain the impedance value constant regardless of the variation of the source voltage amplitude. Many paramaters such as the sampling frequency and the resolution of the ADC/DAC may affect the quality of the output current. The voltage is converted to current using a Howland current source. Several simulations have been performed to visualise the performance of the digital RLC filter.

Finally, the analog and digital programmable RLC impedances are compared in terms of their maximum input voltage, inductance/capacitance range, frequency, ... It will be shown that the digital implementation offers more flexibility to the range of the inductance/capacitance values than the analog impedance.

Unversity of Liège

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1 Introduction

1.1 Motivation and State of art

Simulated loads are crucial if an industry desires to test its power equipment under some specific conditions (fixed inductance range, ...). Those features should provide real world simulation capabilities and prevent overstressing the instrument. Furthermore, a DC/AC electronic impedance plays an essential role in current and future power source testing, especially in the field of renewable energies. Different kinds of loads may be relevant according to the technical specifications :

1. constant power load : the load adjusts its internal impedance to dissipate constant power.
2. constant impedance : two kinds : a resistive impedance and a z impedance which covers the entire complex plane.

A well-known programmable active impedance has been studied and developed by Guan-Chyun Hsieh and Jung-Chien Li[1] in 1993. They suggested an AC active load simulator circuit which can simulate a desired load impedance with a power factor from zero to unity. They employed a software feedback control approach to adjust the current amplitude and the power factor for the purpose of maintaining the impedance value constant regardless of the variation of the source voltage amplitude. The Ph.D of Wei Feng[2] proposes a proper schematic of the inductive/capacitive electronic loads based on the H-bridge dc-dc converter. Another relevant research paper [3] presents a programmable power electronic, constant power load (CPL) using a dc/dc step-up (boost) converter.

Many programmable kinds of impedances have been developed. The LED Load Simulator Model 63110A sold by Chroma[4] can simulate the behaviours of LED's. It contains a programmable interface to model the LED's dynamic resistance. Unfortunately, it's not able to simulate an inductive or capacitive load. Recently, Measurements International developed a programmable impedance simulator which covers the entire complex plane[5].

This feature has been designed to address and fill the need requirement for a better way to calibrate LCR meters. The Z100 model covers the full calibration of LCR meters over simulated impedance from 100 Hz to 20 kHz. The magnitude of the synthesised impedances ranges from 1 Ω to 10 MΩ with an arbitrary phase angle. In the Z1000, the current and the voltage measured by the LCR meter to calculate the impedance are independently generated by two external voltage sources. Adjusting the amplitudes and the relative phase of the voltage sources, the synthesized impedance can cover the entire complex plane. The developers do not reveal more information about the hardware of their product. They only mention that their device is based on a feedback loop in order to control the output current and the phase. One thing is certain, the device is only able to dissipate miliwatts of power and can't be used to simulate the load of a generator.

1.2 Analog Impedance

The first objective is to simulate an analog RLC impedance circuit where the value of the resistor, the capacitor and the inductor are freely chosen by a random user. There are useful circuits for designing a filter or simulating a motor, for example. The user wouldn't have to change physically the inductor component in order to change its value. The same would apply for the capacitor even though digitally controlled variable capacitors are available. For example the NCD2400M[6] component is a digital programmable capacitor which acts like a capacitance decade box. Many capacitors are connected in parallel and some switches are open or closed in order to activate or not the capacitors. Such components won't be used for the rest of the project due to their large step size (coupled to a small available capacitance range).

The phase between the voltage and current should be between [-90°, 90°]. -90° corresponds to a pure capacitor and 90° corresponds to pure inductor. The presence of the resistor changes the phase between -90° and 90°. Adjusting the value of the resistor is easy, a simple analog potentiometer can be used. Furthermore, some digital potentiometers are available and can be controlled via a microcontroller. For the capacitor and the inductor, it's a little bit more complicated. Useful circuits, named gyrators[7], made of operational amplifiers can be used in order to simulate the value of the capacitor or inductor by

adjusting potentiometers[8].

As a first approximation, the op amps are assumed to be ideal:

1. Infinite open-loop gain which doesn't depend on frequency.
2. Infinite input impedance which implies zero input current.
3. Zero input offset voltage.
4. Infinite output voltage range.
5. No output current limitation (this condition limits the range of inductor and capacitor values).
6. Zero output impedance (sometimes not specified in datasheets).
7. Infinite bandwidth with zero-phase shift and infinite slew rate.
8. Zero noise.
9. Infinite common-mode rejection ratio (CMRR).

The circuit that has to be simulated is shown in Fig1.1. It represents a resistor, a capacitor and an inductor connected in parallel whose values can variate. An equivalent RLC series circuit can be derived from this.

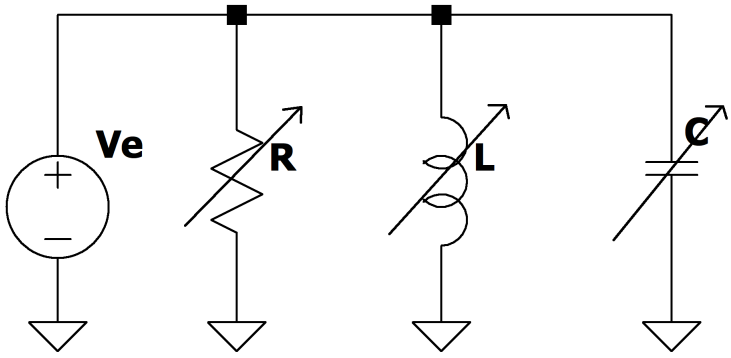

Figure 1.1: RLC parallel impedance

1.3 Digital Impedance

By contrast to the analog impedance, the filtering process is performed digitally. The value of the capacitor and the inductor are adjusted on software. The microcontroller is in charge of computing the output current of the generator. Many parameters may affect the quality of the digital impedance such as

- the sampling frequency (limited by the internal clock of the microcontroller),
- the resolution of the ADC (determined by the number of bits),
- the resolution of the DAC,
- the maximum input voltage of the µC,
- ...

The digital implementation can be modelled using a voltage-controlled current source where the microcontroller is in charge of:

1. Measuring the input voltage thanks to its ADC
2. Computing the output current that should be injected to the generator depending on R, L, C and type of connectivity (parallel or series).
3. Outputting the voltage (image of the output current) to the DAC. This one will be thus converted to current thanks to voltage controlled current source.

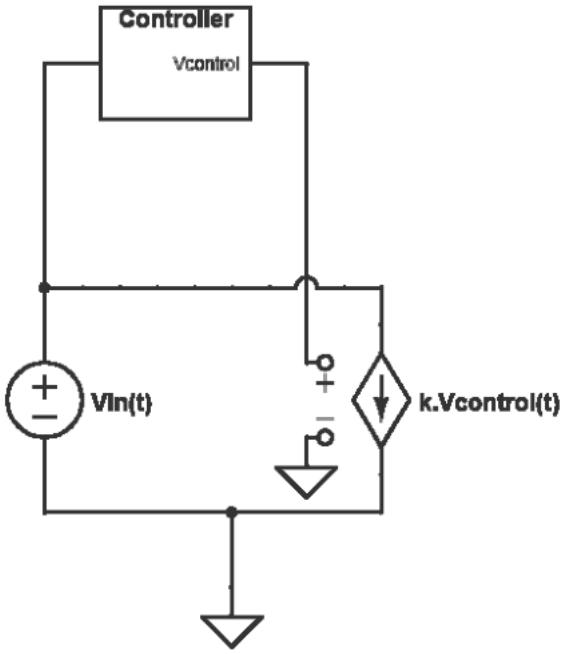

Figure 1.2: Simplified representation of the digital implementation.

The current injected to the generator is controlled by the microcontroller. It's proportional to the current that would flow into an inductor or capacitor.

2 Analog Implementation

2.1 Simulating a variable capacitor with op amps

2.1.1 Non-ideal variable capacitor

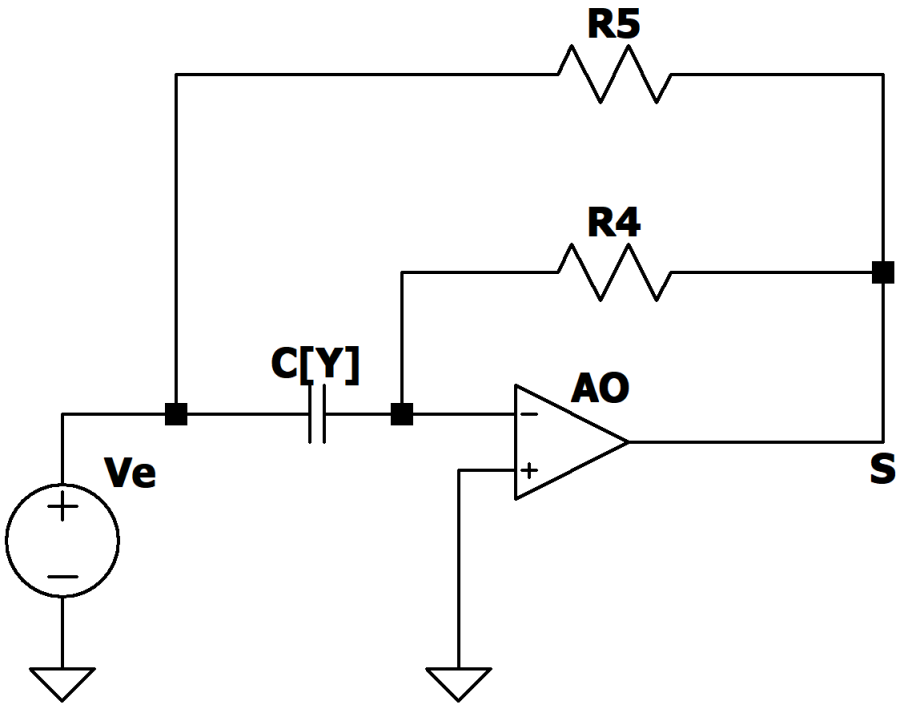

Figure 2.1: Circuit that represents a non-ideal equivalent capacitor which can be adjusted thanks to R_5, R_4 and C.

This circuit is useful in order to simulate an equivalent capacitor C_e from another capacitor C. Let $\hat{Y}$ be the admittance of the capacitor :

$$\hat{Y} = jwC$$

. The equivalent admittance of this circuit can be written as

$$\hat{Y}_e = \frac{\hat{I}_e}{\hat{V}_e}$$

2.1.2 Analysis

Assuming an ideal op amp : $V^+ = V^- = 0V$
$I^+ = I^- = 0 \rightarrow \hat{I}_C = \hat{I}_{R_4}$. The following equations can be easily derived using ohm law across resistors and capacitors :

$$\hat{I}_{R_4} = -\frac{\hat{V}_s}{R_4} = \hat{Y}\hat{V}_e \tag{i}$$

$$\hat{I}_{R_5} = \frac{\hat{V}_e - \hat{V}_s}{R_5} \tag{ii}$$

Injecting (i)→ (ii) :

$$\hat{I}_{R_5} = \hat{I}_{R_4}(\frac{1}{\hat{Y}R_5} + \frac{R_4}{R_5}) \tag{iii}$$

Thus:

$$\hat{I}_{R_5} + \hat{I}_{R_4} = \hat{I}_{R_4}(\frac{1}{\hat{Y}R_5} + \frac{R_4 + R_5}{R_5}) = \hat{I}_e \tag{iv}$$

This way, the input admittance of this circuit is expressed as : $\hat{Y}_e = \frac{1}{R_5} + \hat{Y}(1 + \frac{R_4}{R_5})$. This circuit thus simulates a non ideal capacitor with a resistor R_5 connected in parallel. The expression of the equivalent capacitor is : $C_e = C(1 + \frac{R_4}{R_5})$. The value of the capacitor C_e can be adjusted thanks to a potentiometer R_4 if the resistor R_5 is fixed. R_5 should be chosen sufficiently high in order to decrease as much as possible the value of the parallel resistor and get closer to an "ideal" capacitor. It also limits the output current of the op amp. The dissipation factor(or $\tan(\phi)$) of the non ideal equivalent capacitor is:

$$\tan(\phi) = \frac{1}{wC(R_4 + R_5)}$$

2.1.3 Design of components

As said previously, choosing a large impedance for R_5 allows us to neglect the parallel resistor at high frequency and decrease the output current drawn by the AO. Unfortunately, it decreases the range of available capacitance values.

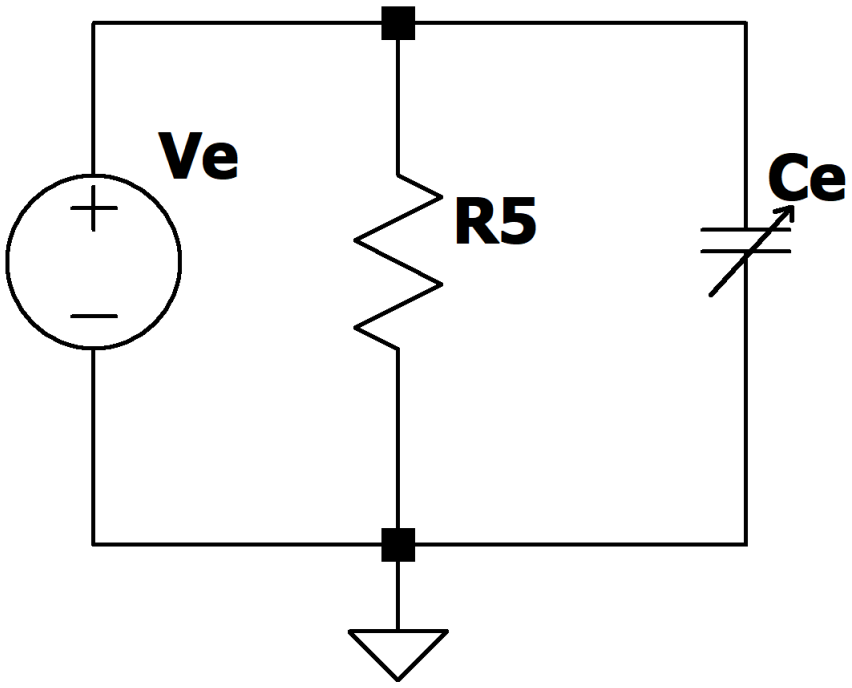

Figure 2.2: Equivalent circuit derived from Fig 2.1

An intuitive approach is adopted here in order to choose the "optimal" values for the resistors and the capacitor. In order to limit as much as possible the output current of the AO ($\hat{I}_s$), the following condition should always be satisfied :

$$|\hat{I}_s|_{max} = |\hat{V}_e(\hat{Y} + \frac{1 + R_4\hat{Y}}{R_5})|_{max} < I_{Lim}$$

Where I_{Lim} is the maximum output current that can be drawn by the AO. R_5 is chosen high (100 kΩ) in order to minimise the dissipation factor. Assuming $|\hat{V}_e|_{max} = 5V$:

$$|\hat{Y} + \frac{1 + R_4\hat{Y}}{R_5}|_{max} < 25^{-1} \text{ (Siemens)}$$

such as the maximum output current can not exceed :

$$\frac{|\hat{V}_e|_{max}(\text{Volt})}{25(\text{Ohm})} = 200\text{mA}$$

It can be shown that the frequency should be less than a certain value depending on R_4 and C :

$$f < \frac{25^{-1}R_5 - 1}{R_5 + R_4}\frac{1}{2\pi C}(\text{Hz})$$

Assuming that R_4 takes values between [10, 100 kΩ], the fundamental frequency of the input voltage should be less than

$$f < \frac{25^{-1}R_5 - 1}{R_5 + R_{4max}}\frac{1}{2\pi C}(\text{Hz})$$
$$f < \frac{3,18 \times 10^{-3}}{C}(\text{Hz})$$

The capacitance value fixes the admissible frequency range.

If Coming back to the expression of the equivalent capacitor :

$$C_e = C(1 + \frac{R_4}{R_5})$$

C_e can only take values between [C, 2C] with respect to R_4 ($\in [10, 100k\Omega]$). Choosing a high value of R_5 unfortunately limits the range of the capacitance.

In the following section it will be studied how this parallel resistor can be removed by connecting in parallel a well-known circuit called : **Negative Impedance Converter (NIC)**.

2.2 Ideal variable capacitor

The best way to remove the parallel resistor to the equivalent capacitor is to connect in parallel a negative impedance to the previous circuit[9]. The absolute value of the negative impedance has to be equal to R_5 in order to cancel its effect. The physics behind a negative impedance is to inject the current drawn by resistor R_5 to the equivalent capacitor from negative impedance $-R_5$.

2.2.1 Negative Impedance Converter (N.I.C)

The concept of the **N.I.C** is introduced using the following circuit:

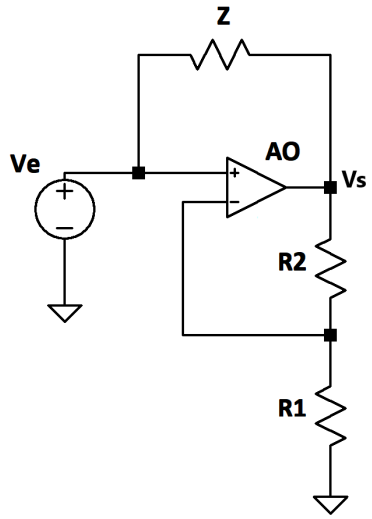

Figure 2.3: Negative Impedance Converter (N.I.C)

The equivalent impedance of this circuit is :

$$\hat{Z}_e = \frac{\hat{V}_e}{\hat{I}_e}$$

The following equations are derived using the Ohm law across the components :

$$\hat{I}_e = \frac{\hat{V}_e - \hat{V}_s}{Z} \tag{i}$$

$$\hat{V}_e = \frac{\hat{V}_s R_1}{R_1 + R_2} \tag{ii}$$

Injecting (ii)→ (i) :

$$\hat{I}_e = \frac{\frac{-\hat{V}_e(R_1+R_2)}{R_1} + \hat{V}_e}{Z} \tag{iii}$$

Thus:

$$\hat{Z}_e = \frac{-ZR_1}{R_2} \tag{iv}$$

The equivalent impedance has to be designed such that it perfectly equals the parallel resistance R_5 in absolute value.

2.2.2 Coupling the N.I.C to the non ideal capacitor

By performing a cut in the pin of the capacitor from fig 2.1, the following circuit is obtained:

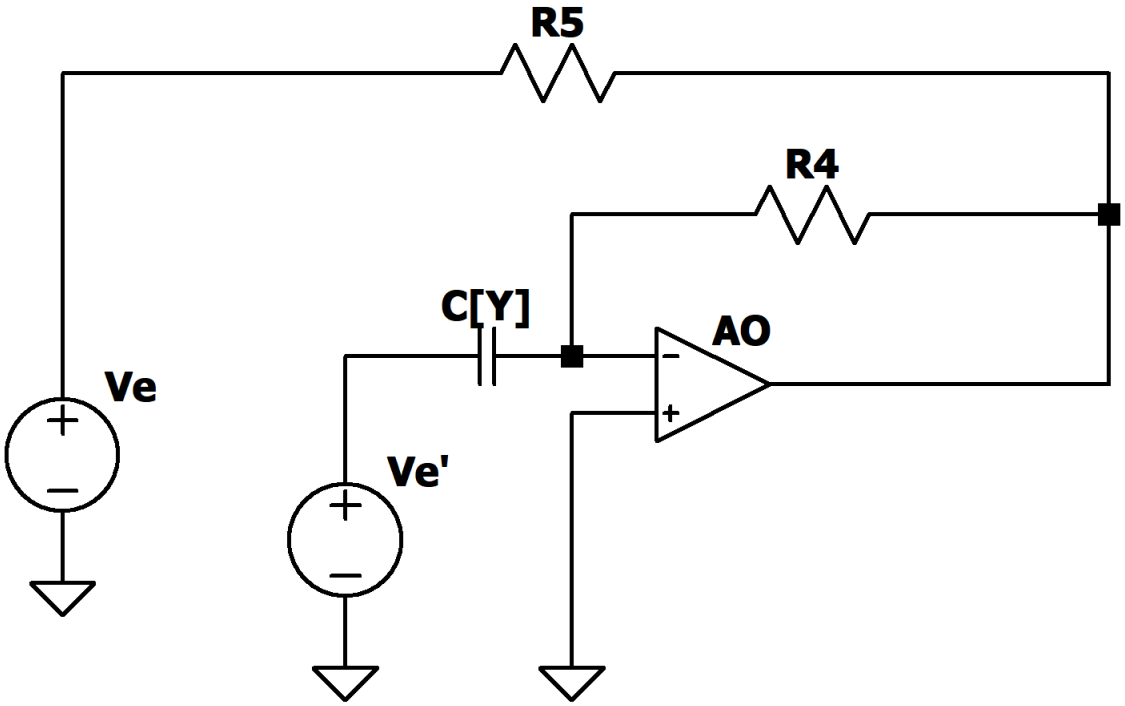

Figure 2.4: Non ideal capacitor circuit from which a cut is performed at the input.

As performed in sub section 2.3, the equivalent admittance can be computed. Let k be the voltage ratio between $\hat{V}_e$ and $\hat{V}_e'$:

$$\hat{I}_{R_4} = -\frac{\hat{V}_s}{R_4} = k\hat{Y}\hat{V}_e \tag{i}$$

$$\hat{I}_{R_5} = \frac{\hat{V}_e - \hat{V}_s}{R_5} \tag{ii}$$

$$\hat{Y}_e = \frac{\hat{I}_{R_5}}{\hat{V}_e} = \frac{\hat{V}_e + k\hat{Y}\frac{\hat{V}_e}{R_4}}{R_5\hat{V}_e} \tag{iii}$$

It results that the equivalent admittance is quite similar to the one derived from section 2.1.1 :

$$\hat{Y}_e = \frac{1}{R_5} + k\hat{Y}\frac{R_4}{R_5}$$

The parallel resistor R_5 is still here, so the objective is to cancel it by connecting a N.I.C in parallel :

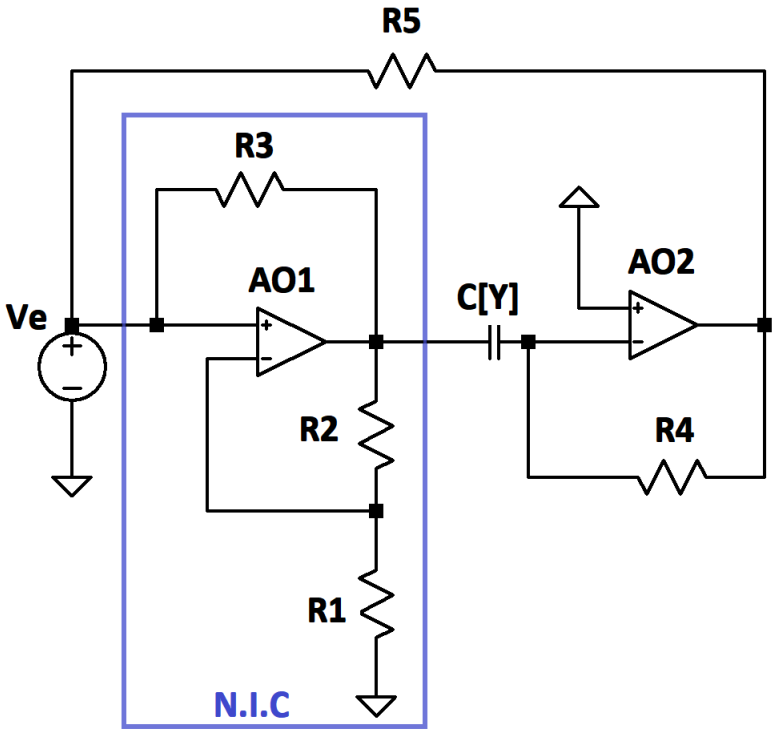

Figure 2.5: Circuit that simulates an "ideal" capacitor using a N.I.C connected in parallel

2.2.3 Analysis

2.2.3.1 Equivalent admittance

The mathematical expression of the equivalent admittance of this circuit can be checked and in which condition it represents a pure capacitor.

$$\hat{Y}_e = \hat{Y}_{e_1} + \hat{Y}_{e_2} \tag{i}$$

Where $\hat{Y}_{e_1}$ is the N.I.C admittance and $\hat{Y}_{e_2}$ is the admittance of the non ideal capacitor.

$$\hat{Y}_{e_1} = -(\frac{R_3 R_1}{R_2})^{-1} \tag{ii}$$

$$\hat{Y}_{e_2} = \frac{1}{R_5} + k\frac{\hat{Y} R_4}{R_5} \tag{iii}$$

Injecting (ii) + (iii) $\rightarrow$ (i) :

$$\hat{Y}_e = \frac{1}{R_5} + k\frac{\hat{Y} R_4}{R_5} - (\frac{R_3 R_1}{R_2})^{-1} \tag{iv}$$

Where $k = \frac{R_1+R_2}{R_1}$

If the following condition is always satisfied :

$$R_5 = \frac{R_3 R_1}{R_2} \tag{v}$$

Then, the redundant resistor is cancelled and the equivalent input admittance corresponds to a pure capacitor :

$$\hat{Y}_e = \frac{R_1 + R_2}{R_1}\frac{\hat{Y} R_4}{R_5} \tag{vi}$$

$$C_e = \frac{R_1 + R_2}{R_1}\frac{R_4 C}{R_5} \tag{vii}$$

If the resistances R_1, R_2, R_3, R_5 are fixed such that condition (v) is satisfied, the equivalent capacitance C_e can be adjusted thanks to a simple potentiometer R_4.

2.2.3.2 AC output current of op amps

Most of op amps are only able to draw a limited output current. It is then a good idea to express the output current of the op amps in terms of surrounding components.

$$\hat{I}_{R_3} = \hat{I}_{S_1} + \hat{I}_C + \hat{I_{R_2}} \tag{i}$$

$$\hat{I}_{R_2} = \frac{\hat{V}_e}{R_1} \tag{ii}$$

$$\hat{V}_{R_2} = \frac{R_2}{R_1}\hat{V}_e + V_e \tag{iii}$$

$$\hat{I}_{R_3} = \frac{\hat{V}_e - \hat{V}_{s_1}}{R_3} \tag{iv}$$

$$\hat{V_{s_1}} = \hat{V}_e(1 + \frac{R_2}{R_1}) \tag{v}$$

$$\hat{I}_C = \hat{V_{s_1}}\hat{Y} \tag{vi}$$

$$\hat{V_{s_2}} = -\hat{I}_C R_4 \tag{vii}$$

$$\hat{I}_{R_5} = \frac{\hat{V}_e - \hat{V}_{s_2}}{R_5} \tag{viii}$$

$$\hat{I_{s_2}} = \hat{I}_{R_5} + \hat{I}_C \tag{ix}$$

Injecting (v) → (iv) :

$$\hat{I_{R_3}} = -\frac{\hat{V}_e R_2}{R_3 R_1} \tag{x}$$

Injecting (v) → (vi) :

$$\hat{I}_C = \hat{V}_e(1 + \frac{R_2}{R_1})\hat{Y} \tag{xi}$$

Injecting (ii) + (x) + (xi) → (i) the output current of the first op amp can be deduced:

$$\hat{I}_{s_1} = -\hat{V}_e(\frac{R_2}{R_3 R_1} + (1 + \frac{R_2}{R_1})\hat{Y} + \frac{1}{R_1}) \tag{xii}$$

Injecting (xi) → (vii) :

$$\hat{V_{s_2}} = -\hat{V}_e(1 + \frac{R_2}{R_1})\hat{Y}R_4 \tag{xiii}$$

(xiii) → (viii) :

$$\hat{I}_{R_5} = \frac{\hat{V}_e + \hat{V}_e(1 + \frac{R_2}{R_1})\hat{Y}R_4}{R_5} \tag{xiv}$$

(xi) + (xiv) → (ix) :

$$\hat{I}_{s_2} = \hat{V}_e\big((1 + \frac{R_2}{R_1})\hat{Y}(1 + \frac{R_4}{R_5}) + \frac{1}{R_5}\big) \tag{xv}$$

2.2.3.3 DC output current of op amps

Since a capacitor is used in this circuit, a constant component of the op amp output current can be superposed to the AC component. The DC component of the output currents of the op amps will be computed. A DC analysis can be performed by assuming a constant voltage across the capacitor (Vc) and no current ($I_C = 0$ A).

Let v(t) be the continuous time voltage across a component, $\hat{v}(t)$ is its AC component (characterised previously by a phasor) and V be its DC component.

It can be easily shown that :

$$\hat{I}_{R_1} = \hat{I}_{R_2} = \frac{V_c}{R_1 + R_2} \tag{i}$$

$$\hat{I}_{R_3} = \frac{V_c}{R_1 + R_2} \tag{ii}$$

The DC output current of the first op amp can be deduced from (i) and (ii) :

$$\hat{I}_{s_1} = I_{R_2} + I_{R_3} = V_c(\frac{1}{R_1 + R_2} + \frac{1}{R_3}) \tag{iii}$$

Now, V_c has to be computed. Let v_c(t) be continuous time voltage across the capacitor, it can be deduced thanks to the Ohm's law that :

$$v_c(t) = v_e(t) + v_e(t)\frac{R_2}{R_1 + R_2} \tag{iv}$$

Assuming that $v_e(t)$ is a pure sine wave with no DC component, then $V_c = 0$ V. As a result, $I_{s_1} = 0$ A.

If a DC analysis is also performed on the second op amp, it can be shown $V_{s_2} = 0$ V because no current flows in the resistor R_4 ($I_{R_4} = 0$ A). Since the DC voltage across R_5 is 0 V, it implies : $I_{R_5} = 0$ A. So the DC component of the output current $i_{s_2}(t)$ is 0 A ($I_{s_2} = 0$ A).

2.2.3.4 Design of components

Short summary :

$$C_e = \frac{R_1 + R_2}{R_1}\frac{R_4}{R_5}C \tag{i}$$

Condition :

$$R_5 = \frac{R_3 R_1}{R_2} \tag{ii}$$

The two current limitations :

$$|\hat{I}_{s_1}| = |\hat{V}_e(\frac{R_2}{R_3 R_1} + (1 + \frac{R_2}{R_1})\hat{Y} + \frac{1}{R_1})| < I_{\text{Lim}} \tag{iii}$$

$$|\hat{I}_{s_2}| = |\hat{V}_e|\big((1 + \frac{R_2}{R_1})\hat{Y}(1 + \frac{R_4}{R_5}) + \frac{1}{R_5}\big)| < I_{\text{Lim}} \tag{iv}$$

The two output voltage limitations :

$$|\hat{V_{s_1}}| = |\hat{V}_e|(1 + \frac{R_2}{R_1}) < V_{\text{sat}} \tag{v}$$

$$|\hat{V_{s_2}}| = |\hat{V}_e|(1 + \frac{R_2}{R_1})|\hat{Y}|R_4 < V_{\text{sat}} \tag{vi}$$

For the sake of simplicity, R_2 is chosen equal to R_1. The condition (ii) then becomes $R_3 = R_5$. The third condition (iii) gives :

$$\hat{I}_{s_1} = \hat{V}_e(\frac{R_2}{R_3 R_1} + (1 + \frac{R_2}{R_1})\hat{Y} + \frac{1}{R_1})$$
$$|\hat{I}_{s_1}| \leq |\hat{V}_e|(\frac{1}{R_3} + 2|\hat{Y}| + \frac{1}{R_1})$$

Making the assumption that the output current I_{Lim} can not exceed 300mA. The resistors should always satisfy these conditions : $R_1 > 50\Omega$, $R_3 > 50\Omega$ and :

$$|\hat{Y}| < 50^{-1}$$

$$wC < 50^{-1}$$

$$f < \frac{1}{50.2\pi C}$$

This way, the AC input current doesn't exceed 300 mA. From the previous expression, it can be seen that the frequency must not exceed a certain value (depending on C) in order to keep the output current under the limit (300 mA taken in the example). The DC component of the output current is not taken into account for the moment.

Adopting the same philosophy for the second op amp concerning the condition (iv) :

$$\hat{I}_{s_2} = \hat{V}_e\big((1+\frac{R_2}{R_1})\hat{Y}(1+\frac{R_4}{R_5})+\frac{1}{R_5}\big)$$
$$|\hat{I}_{s_2}| \leq \hat{V}_e\big((1+\frac{R_2}{R_1})|\hat{Y}|(1+\frac{R_4}{R_5})+\frac{1}{R_5}\big)$$

Choosing $2|\hat{Y}|(1+\frac{R_4}{R_5})+\frac{1}{R_5} \leq 10^{-}1$ allows us to fix the maximum current to 500 mA. it results that :

$$|\hat{Y}| \leq \frac{10^{-1}-\frac{1}{R_5}}{2(1+\frac{R_4}{R_5})}$$
$$wC \leq \frac{10^{-1}-\frac{1}{R_5}}{2(1+\frac{R_4}{R_5})}$$
$$f \leq \frac{10^{-1}-\frac{1}{R_5}}{2.2\pi C(1+\frac{R_4}{R_5})}$$

$R_5$is chosen equal to 5000 Ω in order to let R_4 free to take values between $[50, 1M]$. Taking the most unfavourable case ($R_5 = 5000\Omega$ and $R_4 = 1$ MΩ), the maximum frequency should never exceed 40 kHz.

If C = 1 nF $\rightarrow f_{\max} = 40$ KHz.
Since $C_e = 2\frac{R_4}{R_5}C \in$ [20 pF, 0.4 uF]

2.2.3.5 Output current and output voltage

As said previously, op amps can saturate if the output voltage or the output current is above a certain limit. So, it is interesting to plot those two quantities as a function of the frequency and the equivalent capacitance. It will be easier to determine the available frequency range and capacitance range in order to avoid any voltage or current saturation.

As detailed in the previous section, the resistors R_2 and R_1 are chosen equal. R_5 is fixed to 5000 Ω and R_4 is free to take values between [50 Ω, 1 MΩ].

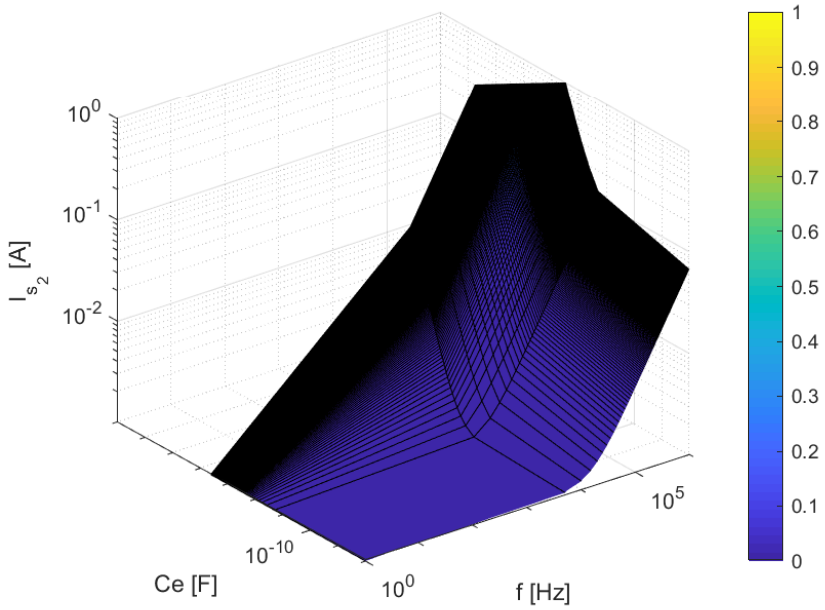

Figure 2.6: Output current (I_{s_2}) of the second op amp with respect to frequency (f) and equivalent capacitance (C_e).

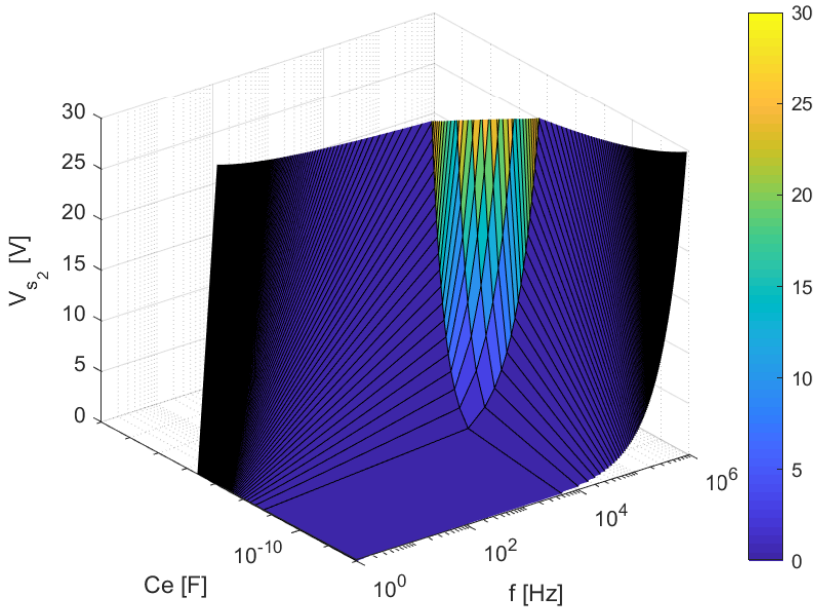

Figure 2.7: Output voltage (V_{s_2}) of the second op amp with respect to frequency (f) and equivalent capacitance (C_e).

As can be seen from these above figures, for a given equivalent capacitance C_e, the output

voltage/current increases with frequency. This is logical since a capacitor behaves like a short-circuit at high frequencies. The choice of the op amp should be optimal such that the available range of capacitance values and frequency is maximised without any saturation.

2.3 Simulating a variable inductor with op amps

2.3.1 Non-ideal variable inductor

Some famous circuits called "gyrators" are able to simulate a non-ideal inductor from op amps.

The circuit has the same architecture as fig 2.1 but the resistor and the capacitor is inverted. It can be shown that the equivalent admittance of this circuit is :

$$\begin{aligned} Y_e &= (1 + \frac{1}{\hat{Y} R_5})\frac{1}{R_4} + \frac{1}{R_5} \\ &= \frac{1}{R_4 R_5 \hat{Y}} + \frac{1}{R_4} + \frac{1}{R_5} \end{aligned}$$

Then the equivalent admittance and parallel resistors can be determined :

$$L_e = R_4 R_5 C$$

in parallel with R_4 and R_5. The equivalent inductance can be adjusted using potentiometers R_4 and R_5 but the parallel resistors change too.

2.3.2 Ideal variable inductor

As performed with the non ideal capacitor, a N.I.C can be connected in parallel to the non ideal inductor in order to remove the parallel resistors.

Analysis

2.3.2.1 Equivalent admittance

Let $\hat{Y}_{e_1}$, $\hat{Y}_{e_2}$ be respectively the admittance of the N.I.C and the gyrator and $\hat{Y}_e$ be the equivalent admittance of the whole circuit.

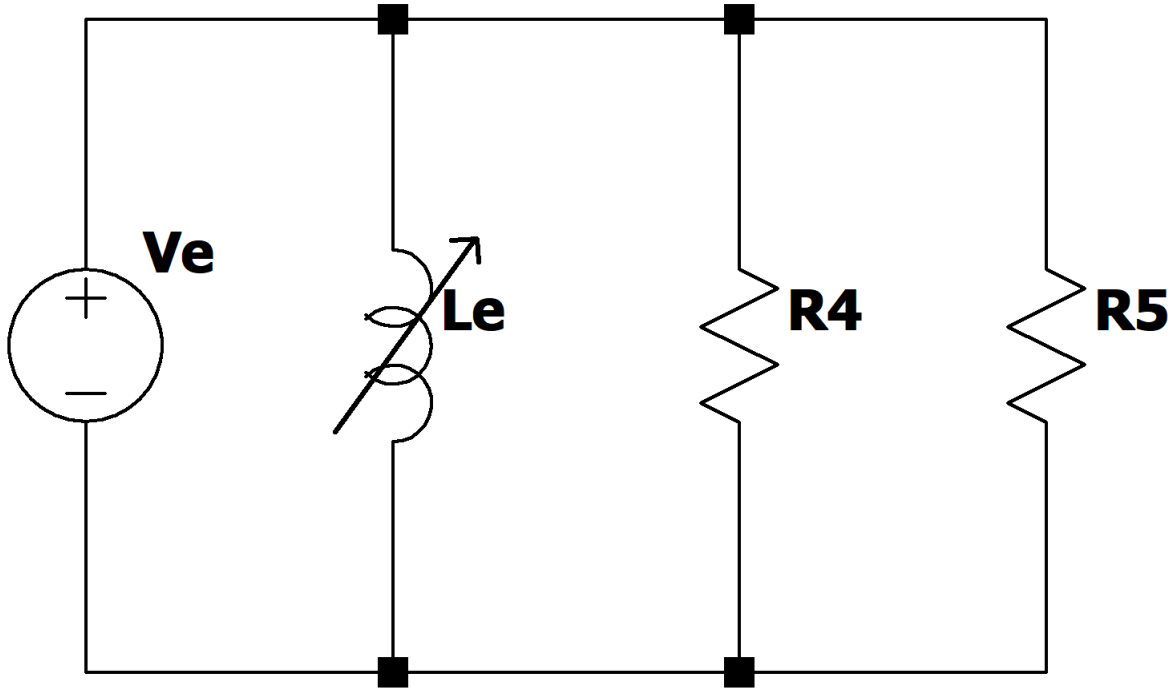

Figure 2.8: Equivalent RL circuit

$$\begin{aligned} Y_e &= Y_{e_1} + Y_{e_2} \\ &= -\frac{R_2}{R_1 R_3} + \frac{1}{R_4} + \frac{1}{R_5} + \frac{1}{R_4 R_5 \hat{Y}} \end{aligned}$$

If the following condition is satisfied :

$$\frac{R_2}{R_1 R_3} = \frac{1}{R_4} + \frac{1}{R_5}$$

the equivalent admittance corresponds to pure inductor :

$$L_e = R_4 R_5 C$$

If the value of the capacitance is fixed, it's possible to adjust the value of the inductance thanks to resistors R_4, R_5.

Furthermore, the op amps are limited in output current. It's thus necessary to make a

more detailed study of the output currents.

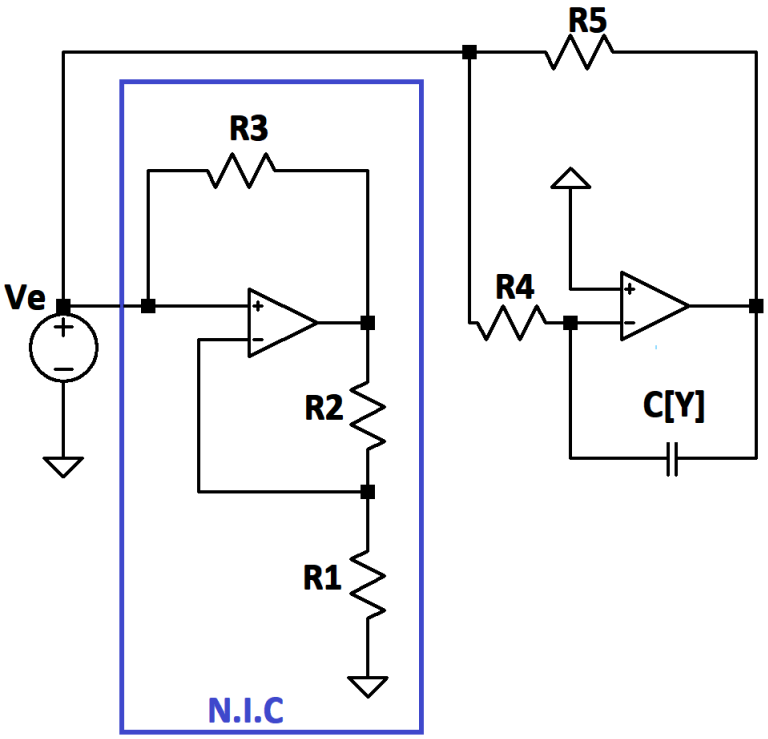

Figure 2.9: Circuit that simulates an ideal inductor by connecting in parallel a N.I.C

2.3.2.2 AC output current of op amps

The AC component of the output current of the op amps will be derived by using phasors for the currents and voltages. The Laplace transform is performed for the capacitor impedance.

$$\hat{I}_{s_1} = \hat{I}_{R_2} - \hat{I}_{R_3} \tag{i}$$

$$\hat{I}_{R_2} = \frac{\hat{V}_e}{R_1} \tag{ii}$$

$$\hat{V}_{R_2} = \hat{I}_{R_2} R_2 \tag{iii}$$

$$\hat{V}_{s_1} = \hat{V}_e + \hat{V}_e \frac{R_2}{R_1} \tag{iv}$$

$$\hat{I}_{R_3} = (\hat{V}_e - \hat{V}_{s_1})/R_3 \tag{v}$$

$$\hat{I}_{R_4} = \hat{V}_e/R_4 \tag{vi}$$

$$\hat{I}_{s_2} = \hat{I}_{R_4} + \hat{I}_{R_5} \tag{vii}$$

Injecting (iv) → (v) :

$$\hat{I_{R_3}} = \big(\hat{V}_e - \hat{V}_e(1 + \frac{R_2}{R_1})\big)/R_3 \tag{viii}$$

(ii) + (viii), the output current of the first op amp can be deduced:

$$\hat{I}_{s_1} = \frac{\hat{V}_e}{R_1}\big(\frac{R_2}{R_3} + 1\big) \tag{ix}$$

$$\hat{I}_{R_5} = \frac{\hat{V}_e - \hat{V}_{s_2}}{R_5} \tag{x}$$

$$\hat{V_{s_2}} = -\frac{\hat{I}_{R_4}}{\hat{Y}} \tag{xi}$$

Injecting (xi) → (x) :

$$\hat{I}_{R_5} = (\hat{V}_e + \frac{\hat{I}_{R_4}}{\hat{Y}})/R_5 \tag{xii}$$

Injecting (vi) + (xii) → (xiii) :

$$\hat{I}_{R_5} = \hat{V}_e\big(\frac{1}{R_5} + \frac{1}{R_4}(\frac{1}{\hat{Y}R_5} + 1)\big) \tag{xiii}$$

(xiii) + (vi) → (vii), the output current of the second op amp can be deduced:

$$\hat{I}_{s_2} = \hat{V}_e(\frac{2}{R_4} + \frac{1}{R_5} + \frac{1}{R_4R_5\hat{Y}}) \tag{xiv}$$

2.3.2.3 DC the output current of op amps

Now, the DC component of the output currents of the operational amplifiers will be derived. A DC analysis can be performed by assuming a constant voltage across the capacitor (V_c) and no current ($I_C = 0$ A).

It results than the output current that is injected in the op amp can only be delivered from the resistor R_5 :

$$I_{R_5} = \frac{V_c}{R_5} = I_{s_2} \tag{i}$$

Where I_{s_2} is the DC component of the output current of the second op amp.

Let $v_c(t)$ be the voltage across the capacitor with $v_c(t) = V_c + \hat{v}_c(t)$. V_c is the DC component and $\hat{v}_c(t)$ the AC component characterised by a phasor (studied in the previous section 4.1.2).

Knowing that :

$$i_c(t) = C\frac{dv_c}{dt} \tag{ii}$$

with $i_c(t) = i_{R_4}(t) = \frac{v_e(t)}{R_4}$

The voltage $v_c(t)$ can be obtained by a simple integration :

$$v_c(t) = \frac{1}{CR_4}\int v_e(t)dt \tag{iii}$$

$$\frac{-1}{CR_4}V_e\frac{cos(wt)}{w} + V_c = v_c(t) \tag{iv}$$

Assuming that the capacitor is initially discharged ($v_c(t = 0) = 0$ V), it can be deduced that

$$V_c = \frac{1}{CR_4}\frac{V_e}{w} \tag{v}$$

From (i), the DC output current of the second op amp can be deduced : (v) $\rightarrow$ (i)

$$I_{s_2} = \frac{1}{CR_4R_5}\frac{V_e}{w} \tag{vi}$$

Concerning the first op amp, it can be easily shown that the DC output current is equal to 0 A.

2.3.2.4 Design of components

Here's a short summary of previous results :

$$L_e = R_4 R_5 C \tag{i}$$

Condition :

$$R_3 = \frac{R_2}{R_1}\frac{R_4 R_5}{R_4 + R_5} \tag{ii}$$

The two current limitations :

$$|\hat{I}_{s_1}| = \frac{|\hat{V}_e|}{R_1}\big(\frac{R_2}{R_3} + 1\big) < I_{\text{Lim}} \tag{iii}$$

$$|\hat{I}_{s_2}| = |\hat{V}_e(\frac{2}{R_4} + \frac{1}{R_5} + \frac{1}{R_4 R_5 \hat{Y}})| < I_{\text{Lim}} \tag{iv}$$

The two output voltage limitations :

$$|\hat{V}_{s_1}| = |\hat{V}_e|(1 + \frac{R_2}{R_1}) \tag{v}$$

$$\hat{V}_{s_2} = \frac{|\hat{V}_e|}{|\hat{Y}|R_4} \tag{vi}$$

Where I_{Lim} is the maximum output current that can be drawn by the op amp.

Choosing $R_2 = R_3$ will always lead to : $|\hat{I}_{s_1}| = 2\frac{|\hat{V}_e|}{R_1}$ (condition (iii)). So the maximum output current of the first op amp is only limited by resistor R_1. The condition (ii) is simplified :

$$\frac{1}{R_1} = \frac{1}{R_4} + \frac{1}{R_5}$$

Concerning the condition (iv), it's a little bit more complicated :

$$|I_{s_2}| \leq |\hat{V}_e|(\frac{2}{R_4} + \frac{1}{R_5} + \frac{1}{R_4 R_5 wC})$$

The output current $|\hat{I}_{s_2}|$ is limited by R_4, R_5 and the admittance wC.

If the available resistance range of R_4, R_5 and the value of the capacitor are well chosen, the condition (iv) can be satisfied for a large frequency range.

If the available values of R_4 and R_5 and the capacitance C are well chosen, the output current limitation (iv) can be satisfied for a large frequency range.

Taking R_4, R_5, $R_5 R_4 wC > 50\ \Omega$ allows to make sure that the output current of the second op amp won't exceed 300 mA :

$$wC \geq \frac{1}{50}$$

$$f \geq \frac{1}{50.2\pi C}$$

Concerning the first op amp, the maximum output current would never exceed 400 mA.

Assuming R_4 takes values between [50, 1MΩ] and $R_5 = 50\Omega$.

If C = 0.1 mF $\rightarrow L_e \in [250m, +\infty]$ with $f_{\min} = 31.8$ Hz.
If C = 10 uF $\rightarrow L_e \in [25m, +\infty]$ with $f_{\min} = 318$ Hz

The DC component of the output current has not been taken into account for the design of components.

2.3.2.5 Output current and output voltage

As said previously, op amps can saturate if the output voltage or the output current is above a certain limit. So, it is interesting to plot those two quantities as a function of the frequency and the equivalent inductance. It will be easier to determine the available frequency range and capacitance range in order to avoid any voltage or current saturation.

R_5 is fixed to 1000 Ω and R_4 is free to take values between [50 Ω, 100 kΩ].

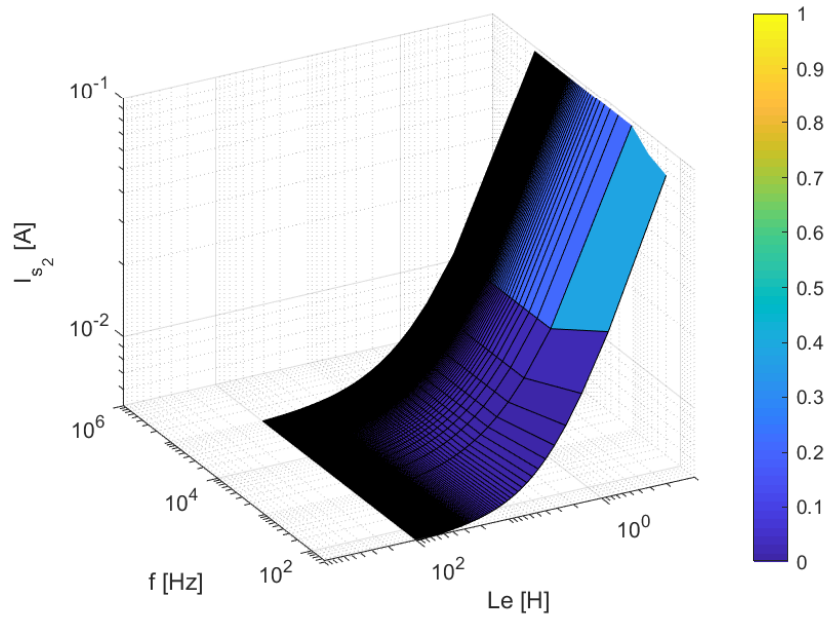

Figure 2.10: Output current (I_{s_2}) of the second op amp with respect to frequency (f) and equivalent inductance (C_e).

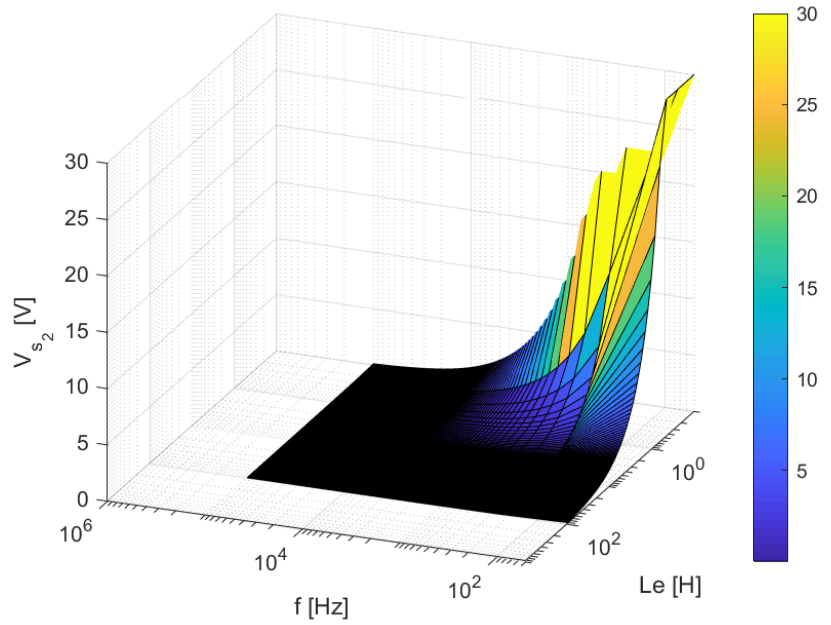

Figure 2.11: Output voltage (V_{s_2}) of the second op amp with respect to frequency (f) and equivalent inductance (C_e).

As can be seen from these above figures, for a given frequency, the output voltage/current is inversely proportional to the inductance. The choice of the op amp should be optimal such that the available range of inductance values and frequency is maximised without

any saturation.

2.4 Spice simulation

2.4.1 Ideal op amps

The following simulations are performed assuming ideal operational amplifiers. The resistors around the op amps and the available range of frequencies are designed such that the output current of the op amps doesn't exceed hundreds of mA's. The software LtSpice[10] is used for simulations.

2.4.1.1 Ideal capacitor simulation

The resistors R_5, R_3 are fixed to 50 Ω in order to let the potentiometer R_4 variate in a large range. The resistors R_2 and R_1 are made equal to 100 kΩ. This way, the N.I.C removes the parallel redundant resistor R_5 as detailed in section 2.

The only parameter that is used to adjust the capacitor is the potentiometer R_4. Let's simulate two random capacitor values : 20 nF and 4 uF. The following formula is used :

$$C_e = 2\frac{R_4}{R_5}C$$

For the following examples, C is chosen equal to 1 nF.

Let's compare these results with a real capacitor connected in parallel with voltage source V_e :

It can clearly be seen that the circuit made of op amps simulates with high accuracy the 20 nF capacitor. Let's change the order of magnitude of the equivalent capacitor to 4 uF by selecting $R_4 = 100$ kΩ.

Lets compare these results with a real 4 uF capacitor connected in parallel with a sine voltage source Ve. The simulated circuit made of op amps replicates exactly the same behaviour as for an ideal 4 uF capacitor. The N.I.C plays a crucial role for simulating an ideal equivalent capacitor depending on the value of the potentiometer R_4 : $C_e = f(R_4)$. It can be noticed that the phase shift between the current source and the voltage source is -90 degrees.

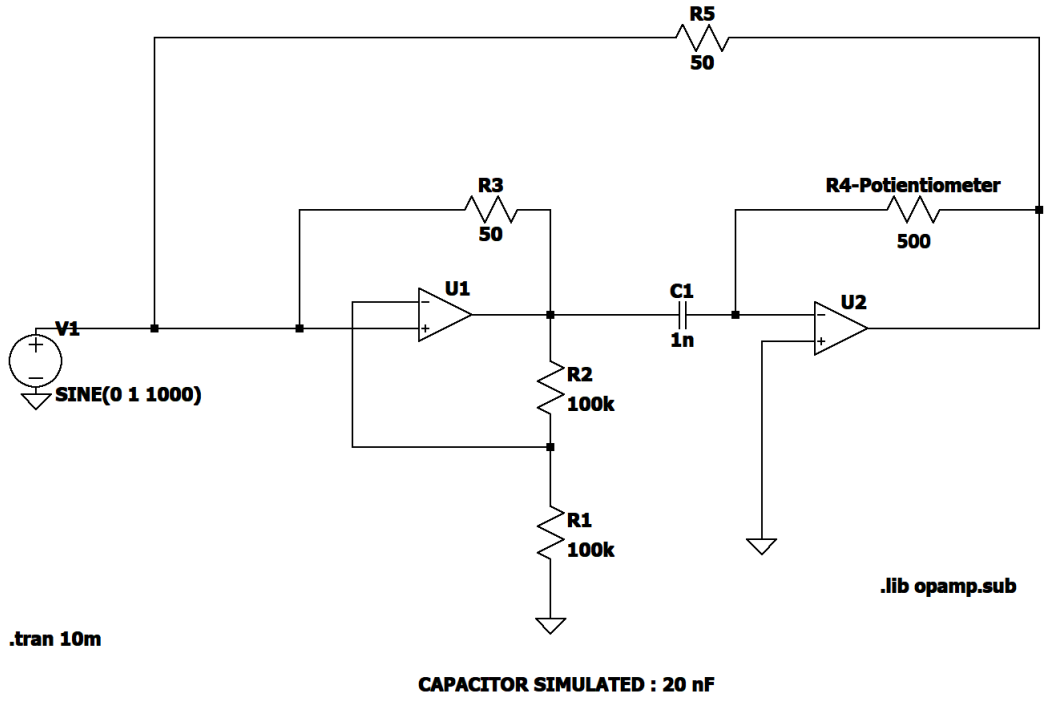

Figure 2.12: Circuit that simulates a 20 nF capacitor.

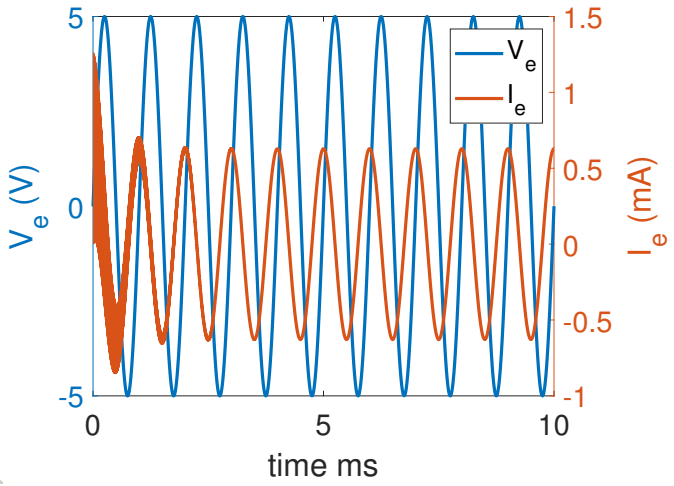

Figure 2.13: Spice simulation : current I_e and voltage V_e for a 20 nF equivalent capacitor C_e.

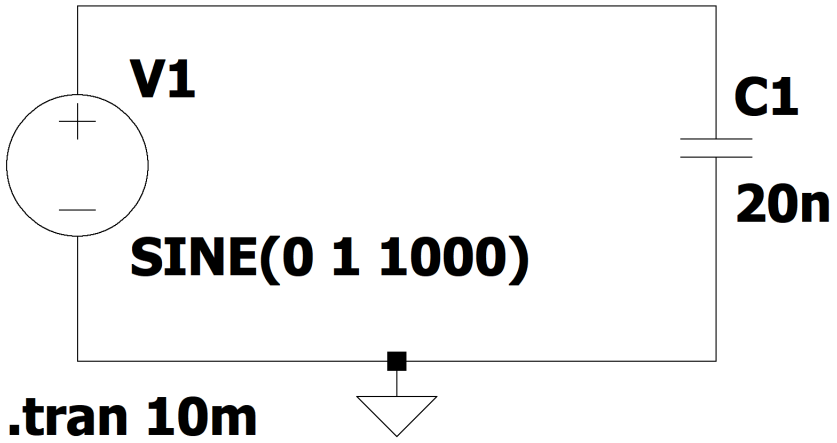

Figure 2.14: Real capacitor 20 nF in parallel with an ideal AC source V_e

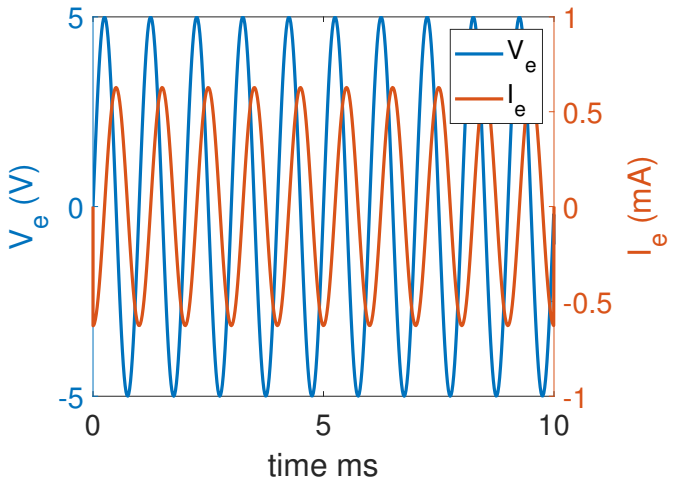

Figure 2.15: Behaviour of the current I_e when a real 20 nF capacitor is connected to an ideal AC source V_e.

2.4.1.2 Ideal inductor simulation

In order to simulate a perfect inductor, the resistors R_3 and R_5 are kept equal to 50 Ω. The value of the inductance can be adjusted using the potentiometer R_5. R_1 is another potentiometer used in order to cancel the parallel resistors. So the following condition must be checked whatever R_4 :

$$\frac{1}{R_1} = \frac{1}{R_4} + \frac{1}{R_5}$$

The equivalent inductor is expressed this way :

$$L_e = R_4 R_5 C$$

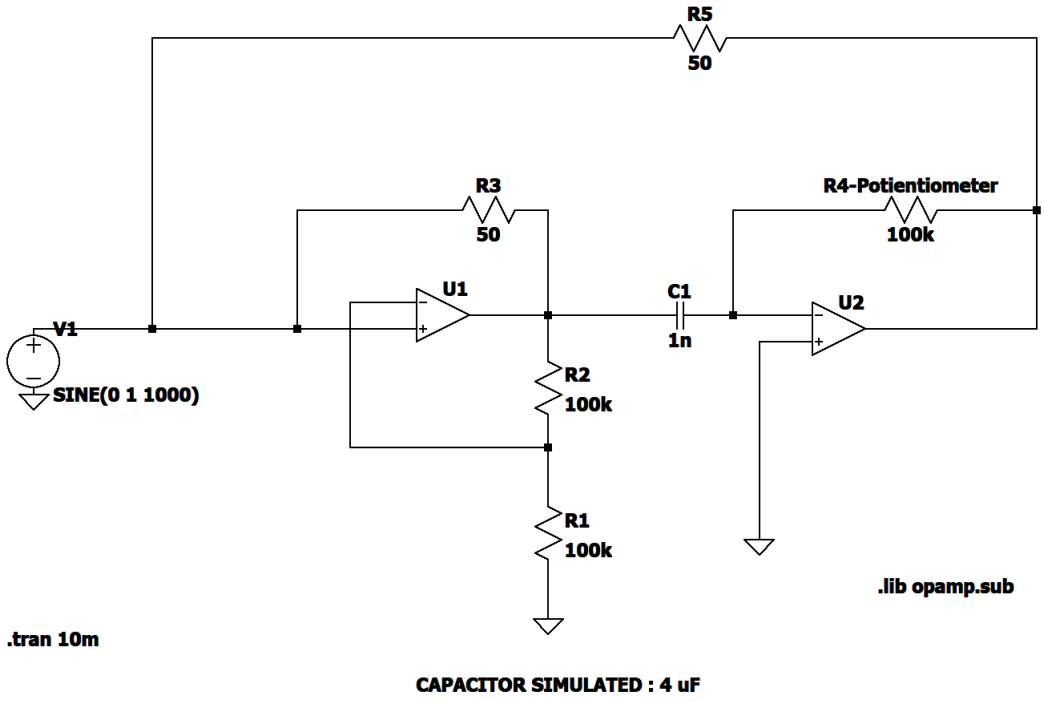

Figure 2.16: Circuit that simulates a 4uF capacitor.

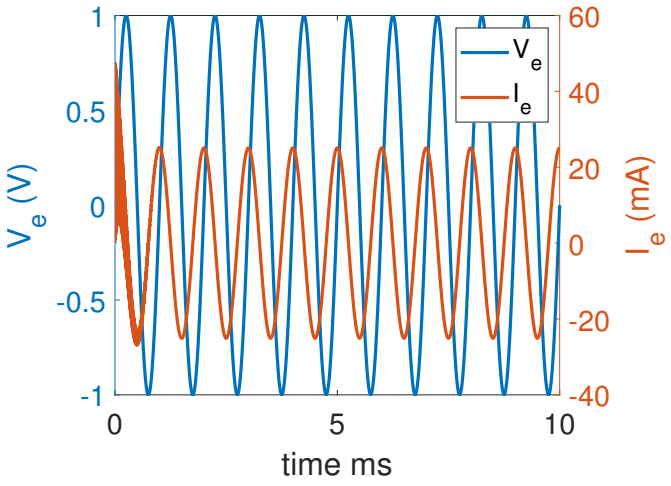

Figure 2.17: Spice simulation : current I_e and voltage V_e for a 4 uF equivalent capacitor C_e.

Let's simulate two random inductor values : 25 mH and 250 mH by adjusting potentiometers R_4 and R_1 :

C is fixed to 10 uF for the following examples.

Let's compare these results to an ideal 25 mH inductor in parallel with an ideal AC source :

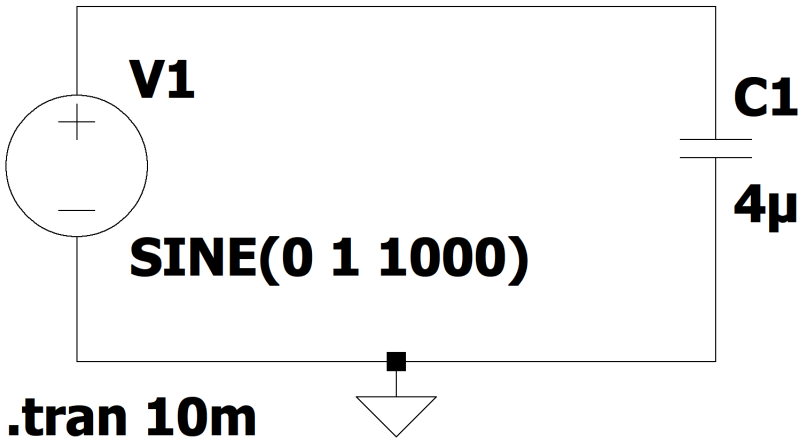

Figure 2.18: Real 4 uF capacitor connected in parallel with an ideal AC source V_e.

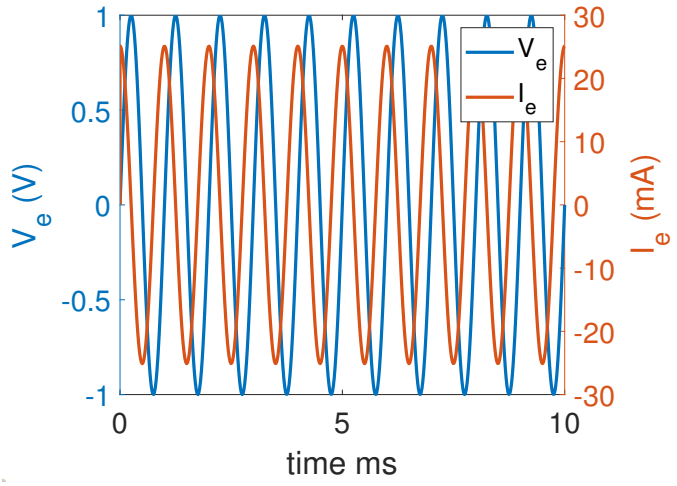

Figure 2.19: Behaviour of the current I_e when a real 4 uF capacitor is connected to an ideal AC source V_e.

As a result, the source current that is going to the equivalent inductor L_e behaves exactly the same way as for an ideal inductor. Let's change the value of the inductor L_e to 250 mH by adjusting R_4 and R_1.

Let's now compare these results to an ideal 250 mH inductor :

As the previous example, the output current I_e of the source is correctly replicated. The phase shift between the current and voltage is 90 degrees.

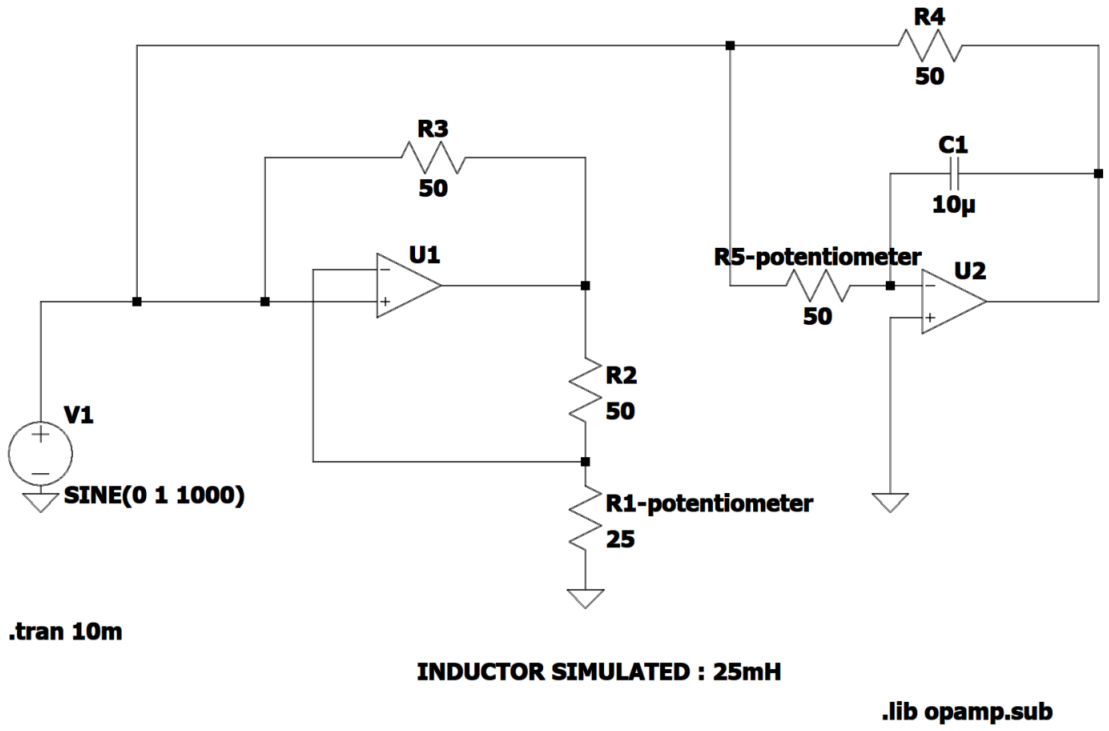

Figure 2.20: Gyrator circuit that simulates a 25 mH inductor.

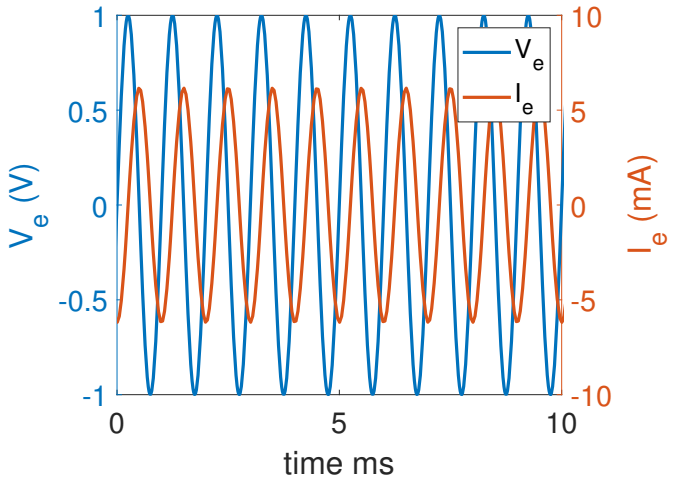

Figure 2.21: Spice simulation : current and voltage I_e and V_e for a 25 mH equivalent inductor L_e.

2.4.2 Real op amp : AD744

The quality of the above circuits can be tested using cheap op amps like the famous AD744[11] characterised by :

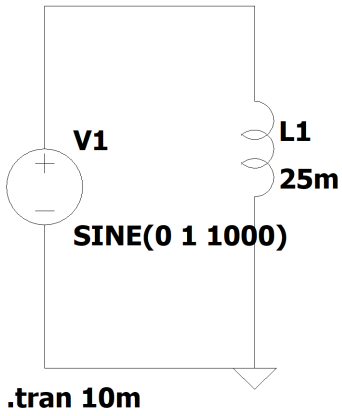

Figure 2.22: Real 25 mH inductor connected in parallel with an ideal AC source V_e.

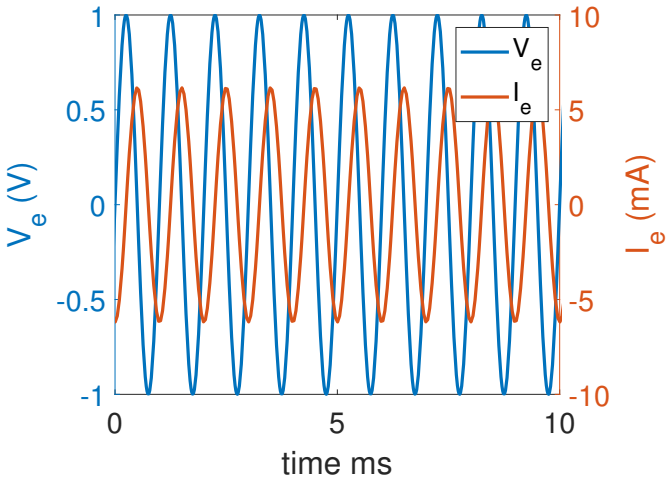

Figure 2.23: Behaviour of the current I_e when a real 25 mH inductor is connected to an ideal AC source V_e.

1. Gain Bandwidth Product : 13 MHz (without any external compensation)

2. CMRR : 88 dB

3. Max dual supply voltage : +/- 18 V

4. Slew rate : 75 V/us

5. Open loop voltage gain : 112 dB

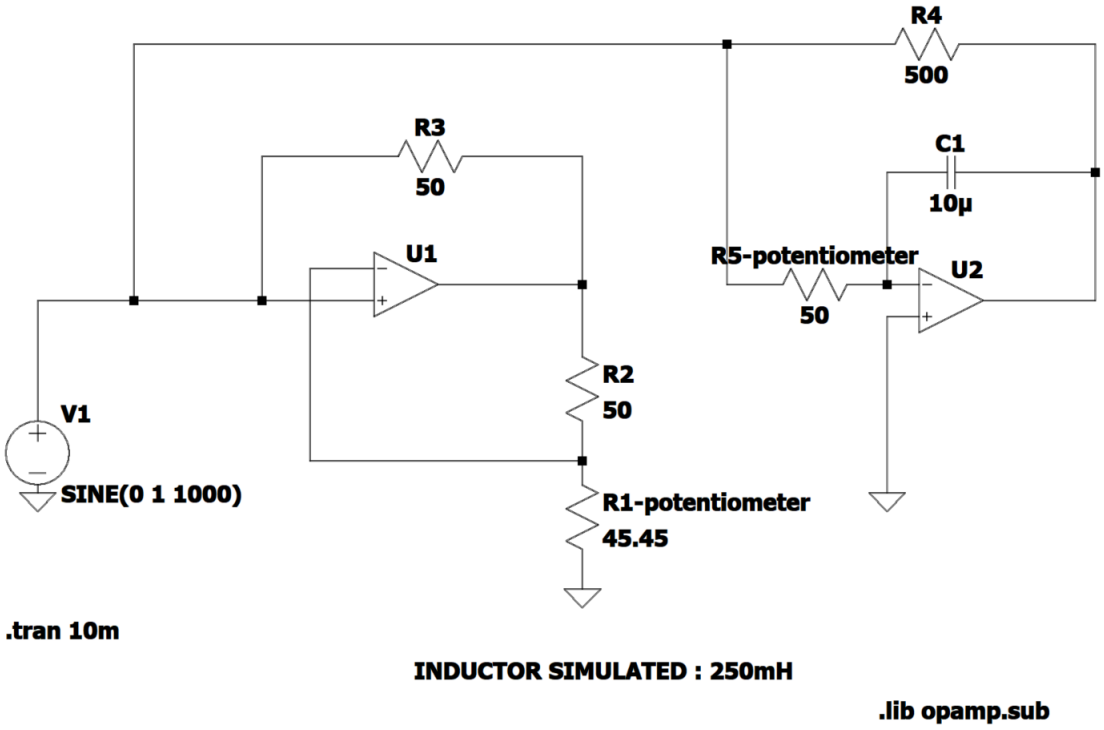

Figure 2.24: Gyrator circuit that simulates a 250 mH inductor.

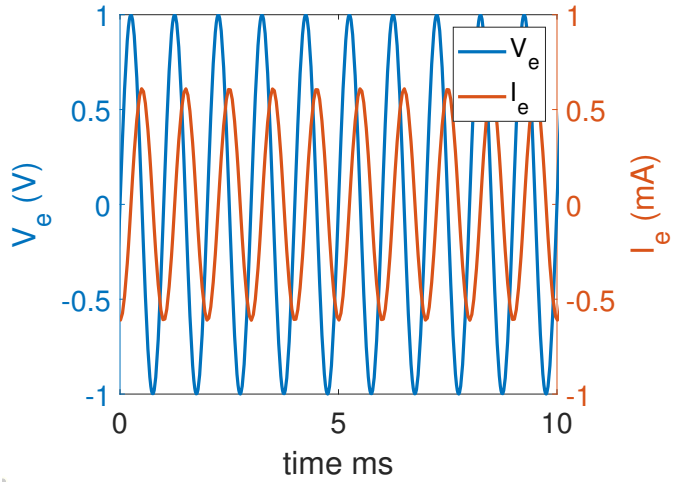

Figure 2.25: Spice simulation : current I_e and voltage V_e for a 250 mH equivalent inductor Le.

6. Max output current : 25 mA (for load of 2 kΩ)

7. Max output voltage : 13 V (for load of 2 kΩ)

The choice of a good operational amplifier with a high gain for a large range of frequencies

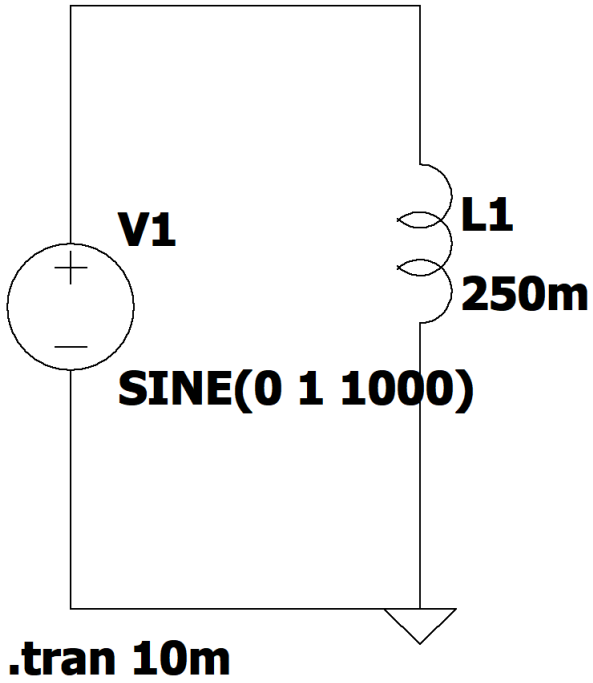

Figure 2.26: Real 250 mH inductor connected in parallel with an ideal AC source V_e.

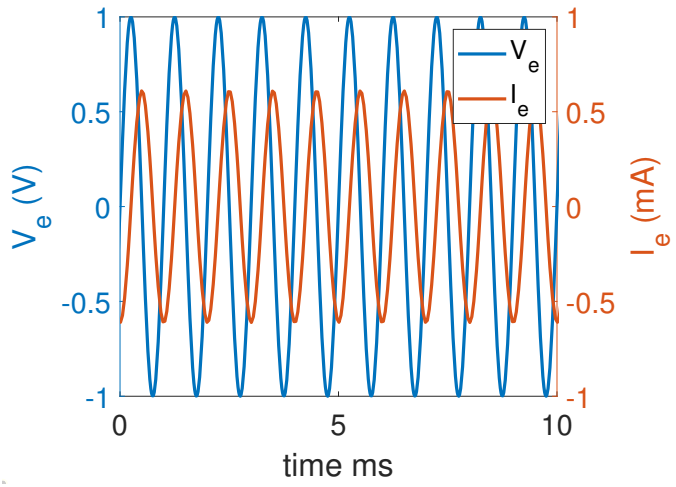

Figure 2.27: Behaviour of the current I_e when a real 250 mH inductor is connected to an ideal AC source V_e.

allows us to take advantage of the negative feedback used in the gyrators and previous circuits (section 3 and 4). The AD744 is highly recommended for designing active filters.

This precision op amp ensures a gain greater than 50 dB until 90 kHz which is suitable for our application (see Fig10 datasheet AD744). Furthermore, The available range

of frequencies can be extended using external compensators. The main limitation are the maximum output current and the output voltage. So the value of the components around the op amps have to be adjusted such that these limitations are satisfied.

2.4.2.1 Ideal capacitor simulation

design of components Based on the results provided in section 2.2.3.4, R_2 is chosen equal to R_1. This implies that R_3 must be equal to R_5 in order to cancel the redundant parallel resistor thanks to the N.I.C. Choosing R_3 and R_1 greater than 5000 Ω and $|\hat{Y}| \leq \frac{1}{5000}$ allows us to fix the maximum output current of the first op amp to 4 mA. This is an upper bound that has been exaggerated in order to be sure that the output current is of the order of 20 mA. We'll compute later the true maximum once the value of the capacitor will be fixed.

The frequency should be

$$f \leq \frac{1}{500.2\pi C}$$

As a reminder, the equivalent capacitance is $C_e = 2\frac{R_4}{R_5}C$

Concerning the second op amp, If we let R_4 going from 50 to 50 kΩ, the following condition ensures that the maximum output current never exceeds 25 mA (exaggerated as mentioned previously) :

$$f \leq \frac{5 \times 10^{-3} - \frac{1}{R_5}}{2.2\pi C(1 + \frac{R_4}{R_5})}$$

Choosing a capacitance value C = 1 nF allows us to work with a maximum frequency of 18 kHz in order to satisfy the output current limitation of the op amp. The capacitance value can take values on the range : [20 pF, 20 nF]. The potentiometer R_4 is used in order to adjust the equivalent capacitance.

Furthermore, the output voltage of the AD744 is also limited. So the maximum allowed frequency is less than 18 Khz. As determined in section 2.2.3.4 (vi), the maximum output voltage of the op amp should be less than 18 V (saturation voltage):

$$|\hat{V_{s_2}}| = |\hat{V_e}|(1 + \frac{R_2}{R_1})|\hat{Y}|R_4 < 18 \text{ V}$$

$$f < \frac{18}{2|\hat{V_e}|R_4 2\pi C}$$

$$f < 5730 \text{ Hz}$$

So the maximum allowed frequency is in the order of 5 kHz in order to avoid any voltage saturation of the AD744. This is confirmed by simulation in LT spice.

Spice Simulation of an adjustable capacitor Let's simulate the following capacitance and compare it with a real capacitor. The simulation is performed for a 2 nF and a 20 nF equivalent capacitor.

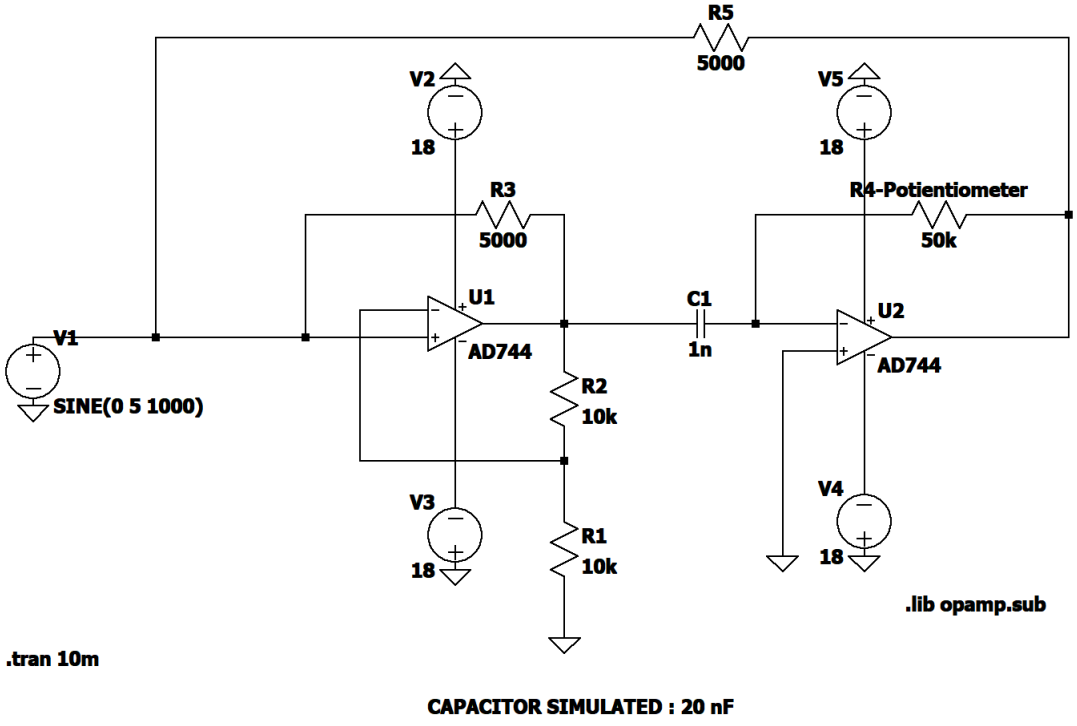

Figure 2.28: Circuit that simulates a 20 nF capacitor using ad744 op amp

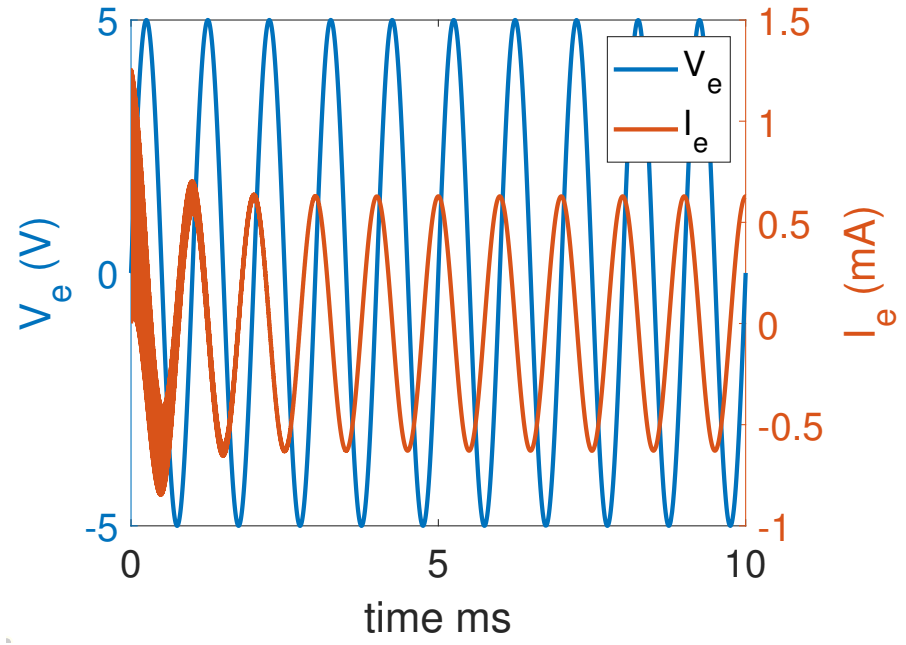

Figure 2.29: Spice simulation : current I_e and voltage V_e for a 20 nF equivalent capacitor C_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

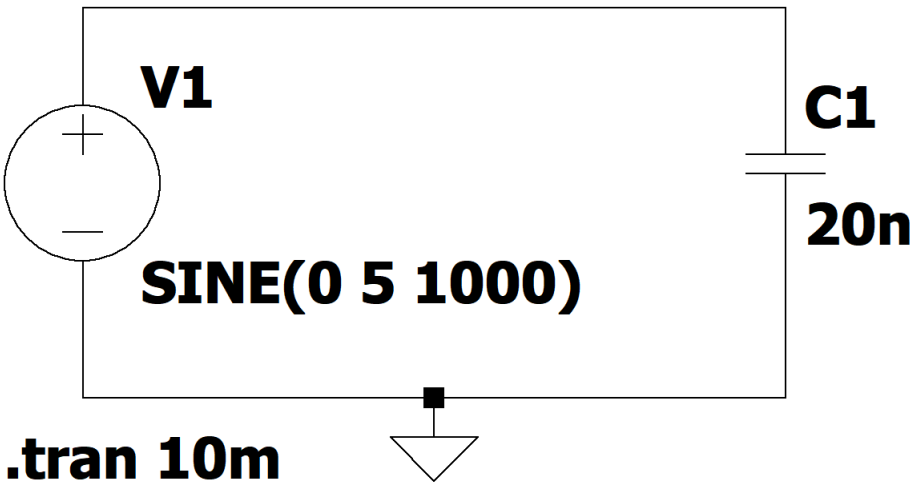

Figure 2.30: Circuit that simulates a real 20 nF capacitor.

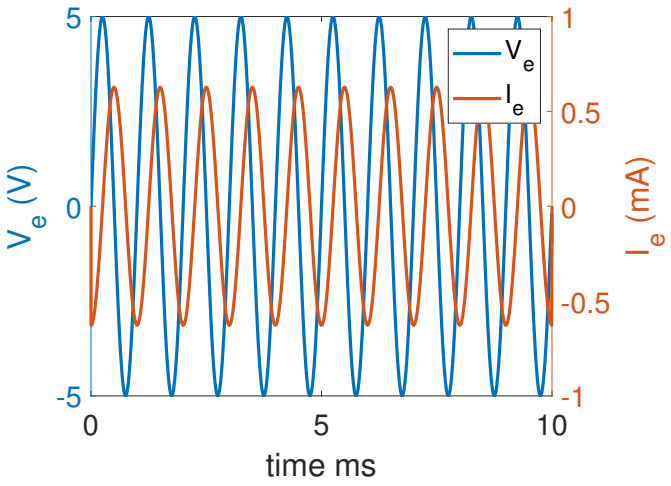

Figure 2.31: Spice simulation : current I_e and voltage V_e for a real 20 nF capacitor C_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

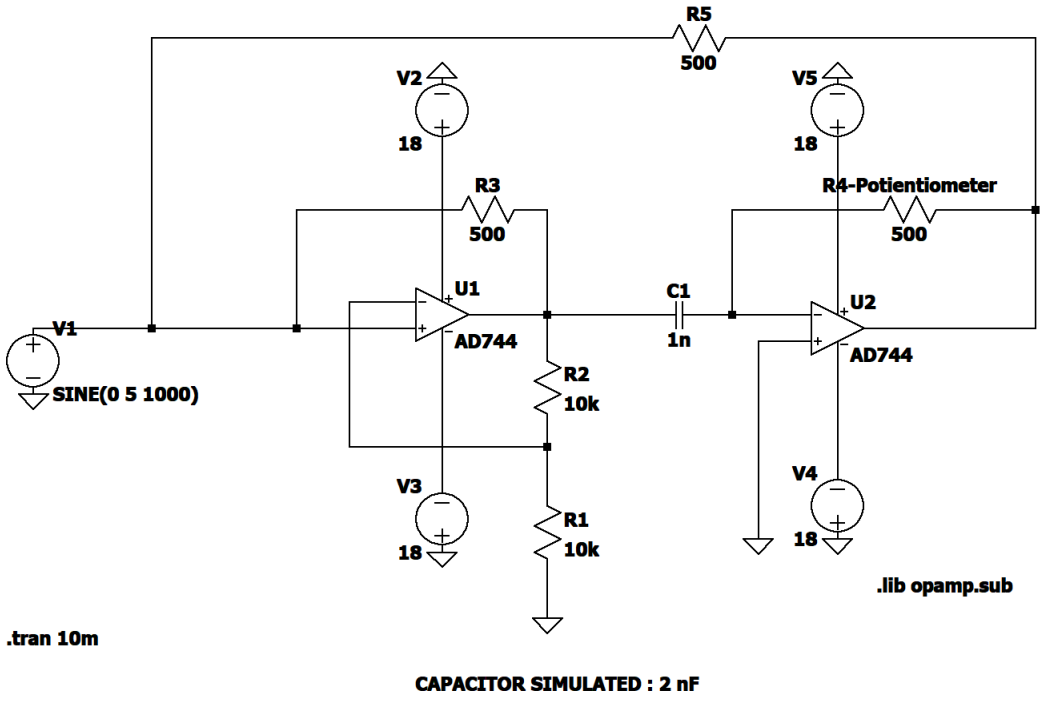

Figure 2.32: Circuit that simulates a 2 nF equivalent capacitor using AD744 op amps.

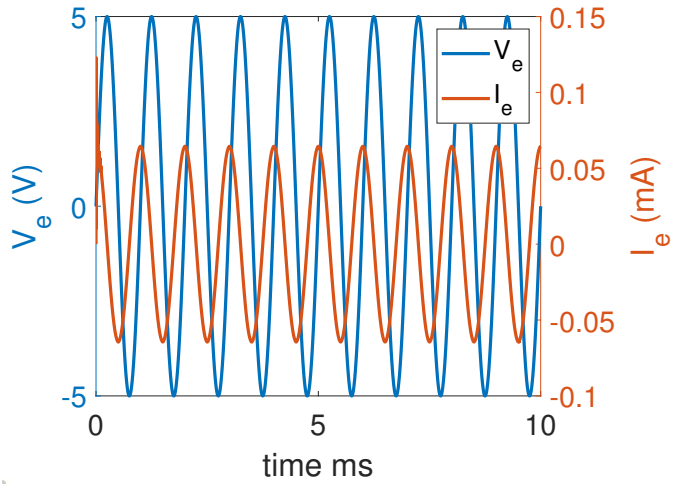

Figure 2.33: Spice simulation : current I_e and voltage V_e for a 2 nF equivalent capacitor C_e. The input voltage is a sinus of frequency 1000 Hz. The op amp is the AD744.

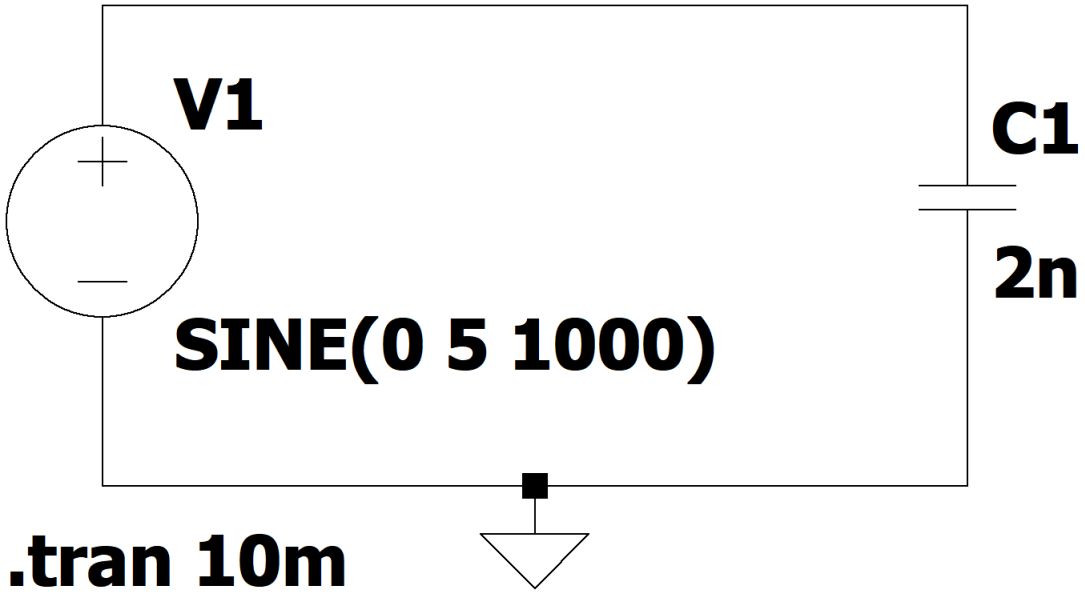

Figure 2.34: Circuit that simulates a 2 nF real capacitor.

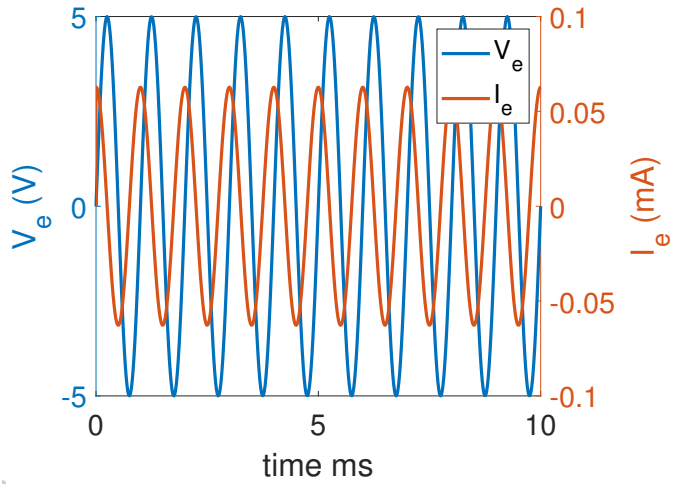

Figure 2.35: Spice simulation : current I_e and voltage V_e for a real 2 nF capacitor C_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

2.4.2.2 Ideal inductor simulation

design of components For the sake of simplicity, the resistors R_2 and R_3 are kept equal. It results that the following condition must always be satisfied whatever the value of the potentiometer R_4 :

$$\frac{1}{R_1} = \frac{1}{R_4} + \frac{1}{R_5}$$

So R_1 has to be permanently adjusted in order to cancel the parallel resistor term. Choosing R_4 and R_5 greater than 1000 kΩ allows us to fix the maximum output current of the first op amp to 20 mA.

Concerning the second op amp, the fundamental frequency of the input signal must be greater than a certain threshold in order to make sure that the output current doesn't exceed 20 mA :

$$f \geq \frac{1}{1000.2\pi C}$$

As a reminder : $L = R_4 R_5 C$

Choosing C = 1 uF allows us to have an inductor that ranges from [1, 100H] with a minimum input frequency of 159 Hz.

Furthermore, the output voltage of the second op amp should stay under its limitation :

$$|\hat{V}_{s_2}| = \frac{V_e}{R_4|\hat{Y}|} < 18 \text{ V}$$

$$f > \frac{V_e}{R_4 2\pi C}\frac{1}{18}$$

$$f > 44 \text{ Hz}$$

Spice Simulation of an adjustable inductor As performed for the equivalent capacitor, the AD744 is used in order to simulate the gyrator. We assume a sinus input voltage at 1000 Hz. Two inductor values are simulated : 1 Henry and 100 Henry. The performance of the gyrator is compared with ideal inductors.

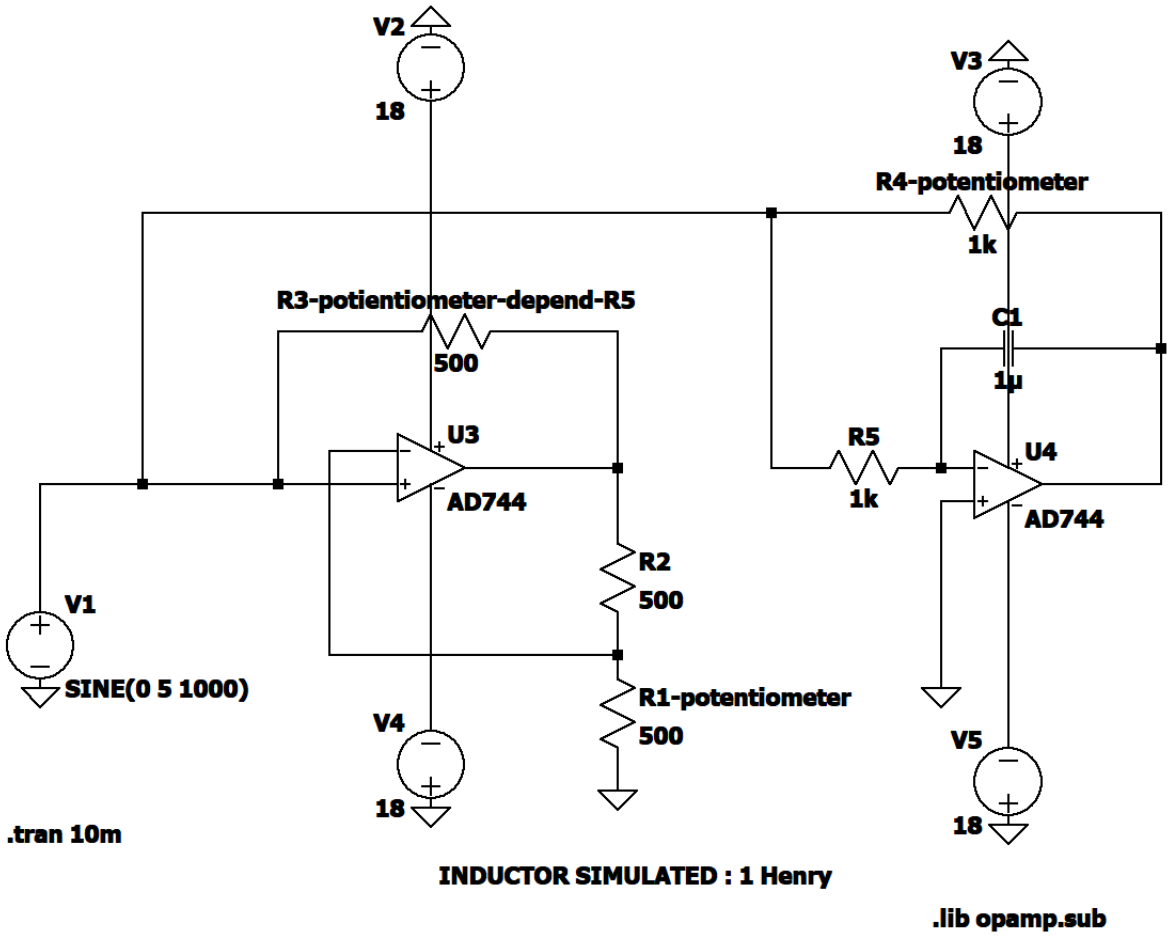

Figure 2.36: Circuit that simulates a 1 henry equivalent inductor.

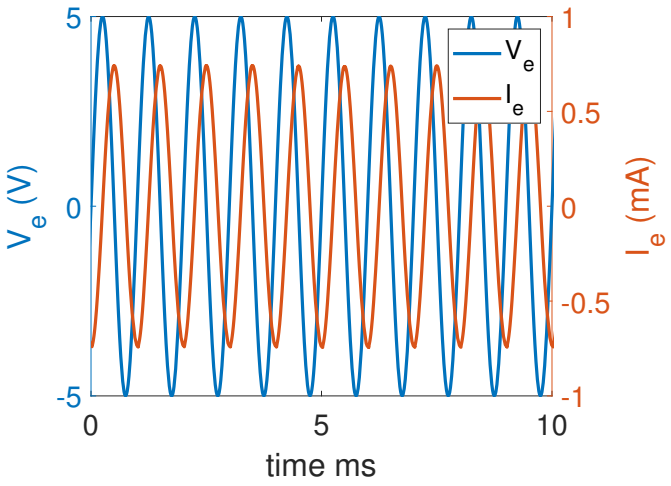

Figure 2.37: Spice simulation : current I_e and voltage V_e for a real 1 Henry inductor L_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

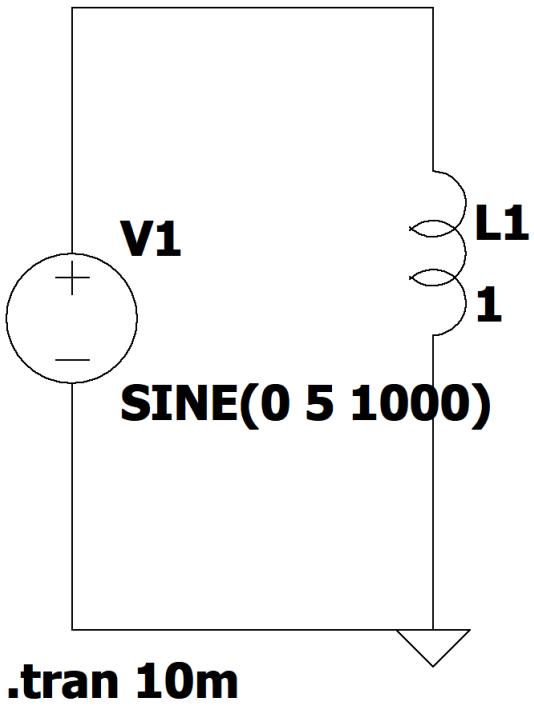

Figure 2.38: Circuit that simulates a 1 Henry ideal inductor.

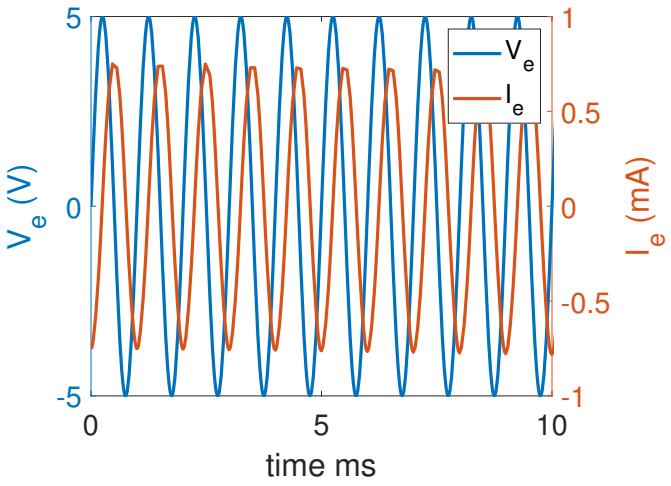

Figure 2.39: Spice simulation : current I_e and voltage V_e for an ideal 1 Henry capacitor L_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

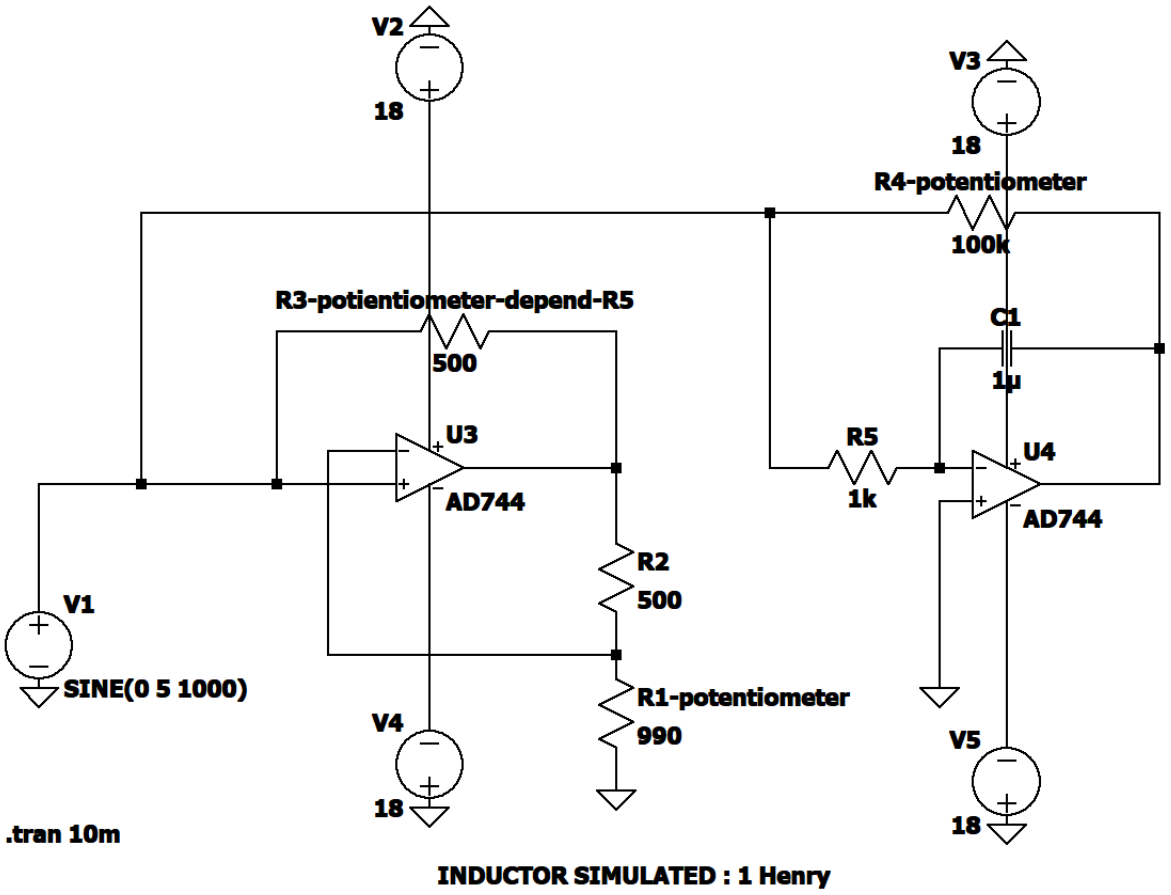

Figure 2.40: Circuit that simulates a 100 henry equivalent inductor.

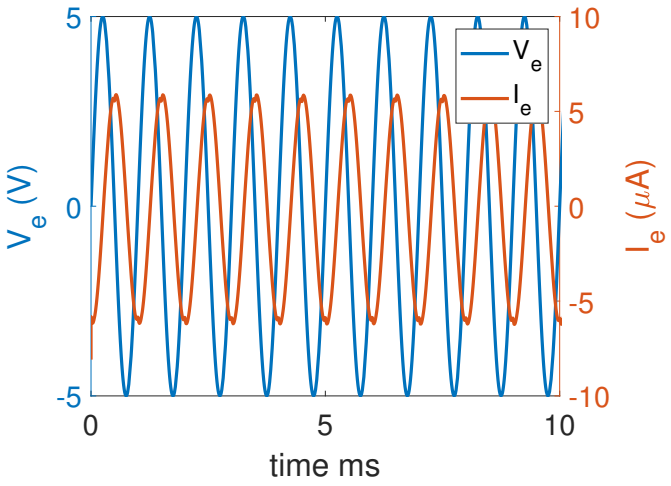

Figure 2.41: Spice simulation : current I_e and voltage V_e for an equivalent 100 Henry inductor L_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz

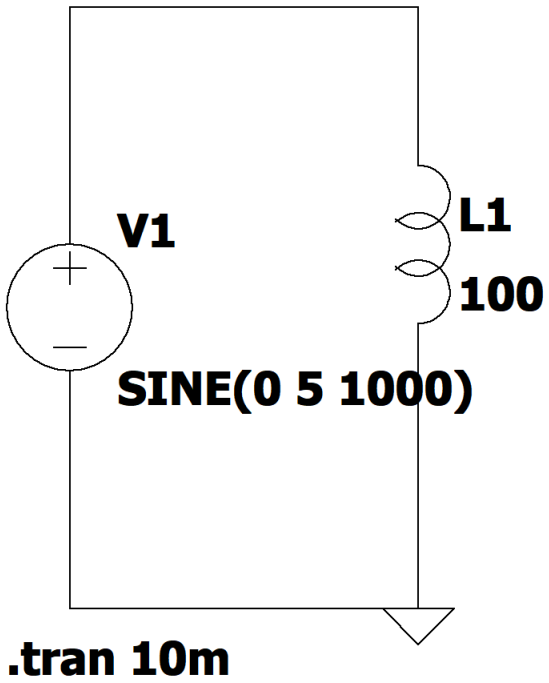

Figure 2.42: Circuit that simulates a 100 Henry ideal inductor.

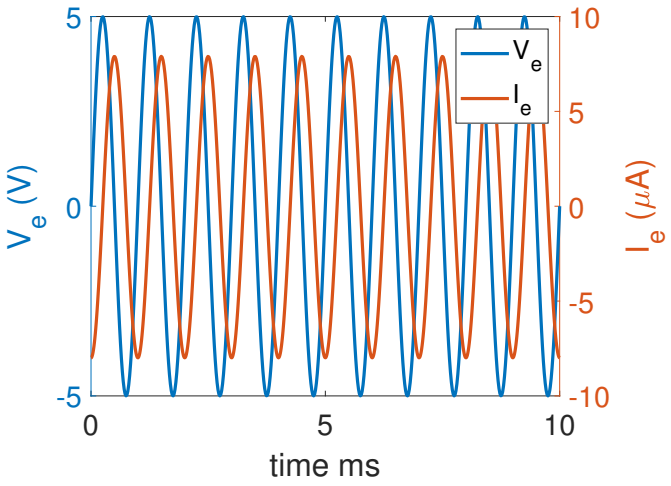

Figure 2.43: Spice simulation : current I_e and voltage V_e for an ideal 100 Henry capacitor L_e. The input voltage is a sinus of amplitude 5V and of frequency 1000 Hz.

2.4.2.3 RLC impedance simulation

As a short summary, it's possible to simulate a RLC impedance using the AD744 op amps with the following characteristics :

- R ∈ [1, 100 kΩ]
- C ∈ [20 pF, 20 nF]
- L ∈ [1, 100H]
- f ∈ [159 Hz, 5.7 kHz]
- 0V < V_{in} < 5V

NB : the capacitors are assumed to be ideal (ESR = 0 Ω) The idea is to combine the gyrator and the capacitor equivalent circuit in order to simulate an "ideal RLC impedance" by adjusting simple potentiometers.

Let's simulate a RLC impedance with :

1. R = 1 kΩ
2. C_e = 2 nF
3. L_e = 2 Henry

4. Input voltage of 5 V of frequency 5000 Hz.

As a reminder, the equivalent capacitance is determined by this expression :

$$C_e = 2\frac{R_4}{R_5}C$$

And the equivalent inductance by this expression :

$$L_e = R'_4 R'_5 C'$$

But the following condition should always be satisfied in order to cancel the redundant parallel resistors :

$$\frac{1}{R_1} = \frac{1}{R_4} + \frac{1}{R_5}$$

R_4 is thus adjusted to 5000 Ω in order to have $C_e = 2$ nF and $R'_4 = 2$ kΩ with $R_1 = 666$ Ω in order to get $L_e = 2$ H.

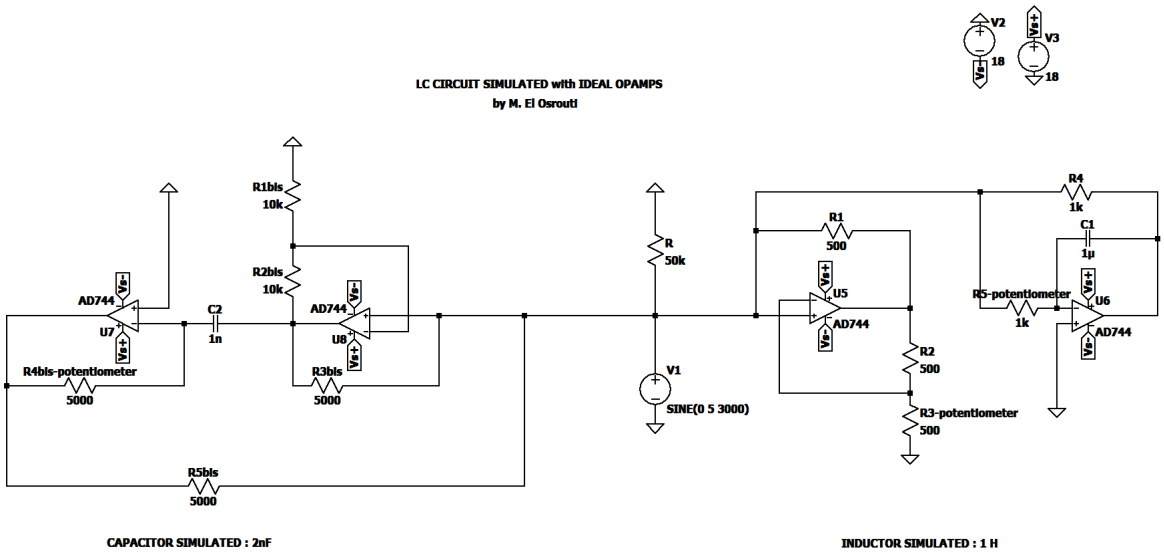

Figure 2.44: RLC impedance simulated using the ad744 op amps. The amplitude of the sinus input voltage V_e is set to 5V and the corresponding frequency is 3000 Hz. $L_e = 1$ H, $C_e = 2$ nF and R = 50 kΩ.

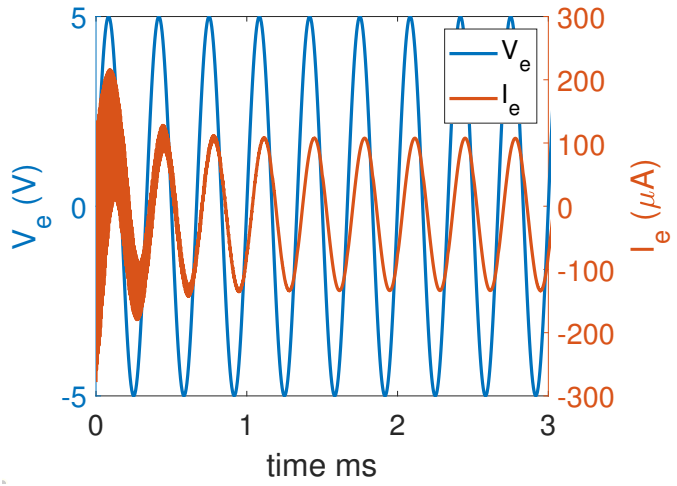

Figure 2.45: Spice simulation : current I_e and voltage V_e for $Le = 1$ H, $C_e = 2$ nF and R = 50 kΩ. The input voltage is a sinus of amplitude 5V and of frequency 3000 Hz.

There is a small transient response for the simulated RLC impedance. After 0.3 ms, the high frequency oscillation is attenuated. The performance of the RLC impedance made of op amps can be compared to an ideal RLC impedance.

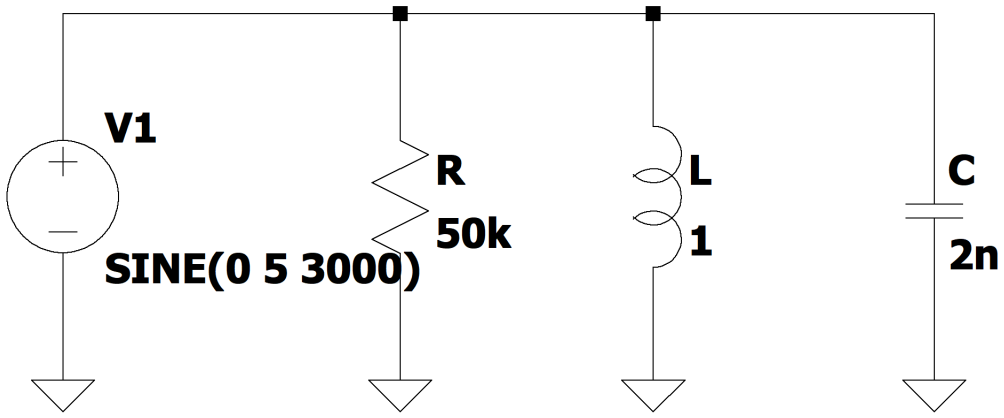

Figure 2.46: ideal RLC impedance with $L = 2$ H, $C = 2$ nF and R = 1 kΩ.

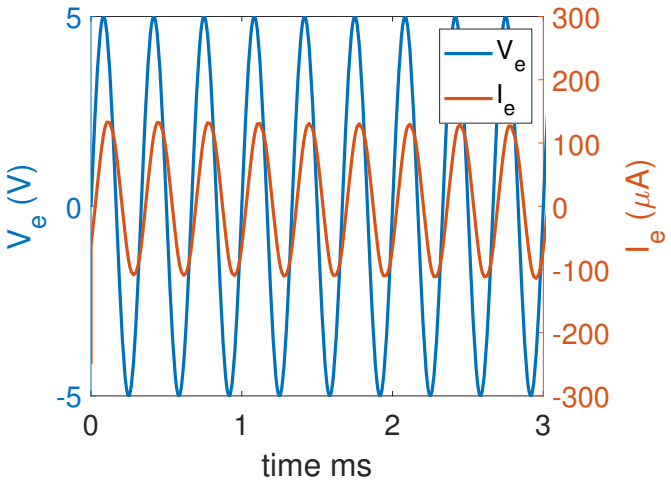

Figure 2.47: Spice simulation : current I_e and voltage V_e for $L = 2$ H, $C = 2$ nF and R $= 1$ kΩ. The input voltage is a sinus of amplitude 5V and of frequency 5000 Hz.

As can be observed in plot 4.34 and plot 4.36, the two outputs current delivered by the source V_e share the same global behaviour. The peak output current is around 5 mA. And the phase shift between the voltage and current is the same.

2.4.2.4 Switched RC-RL impedance

In some applications, simulating a RLC parallel impedance is not useful. By using a switch between the RC and RL impedance, the user is free to simulate either an inductive (in case of a motor for example) or a capacitive impedance. This will allow the user to increase the available bandwidth frequency without risk of saturation of the op amps. If the user tries to simulate a RC capacitive load, he will only be limited at high frequencies (risk of voltage saturation of the opamp since the ideal capacitor would act as a "short-circuit"). But he won't be limited at low frequencies. On the other hand, if the user desires to simulate an RL inductive load, he will only be limited at low frequencies (risk of current saturation at very low frequencies since the ideal parallel inductor would act like a "short-circuit").

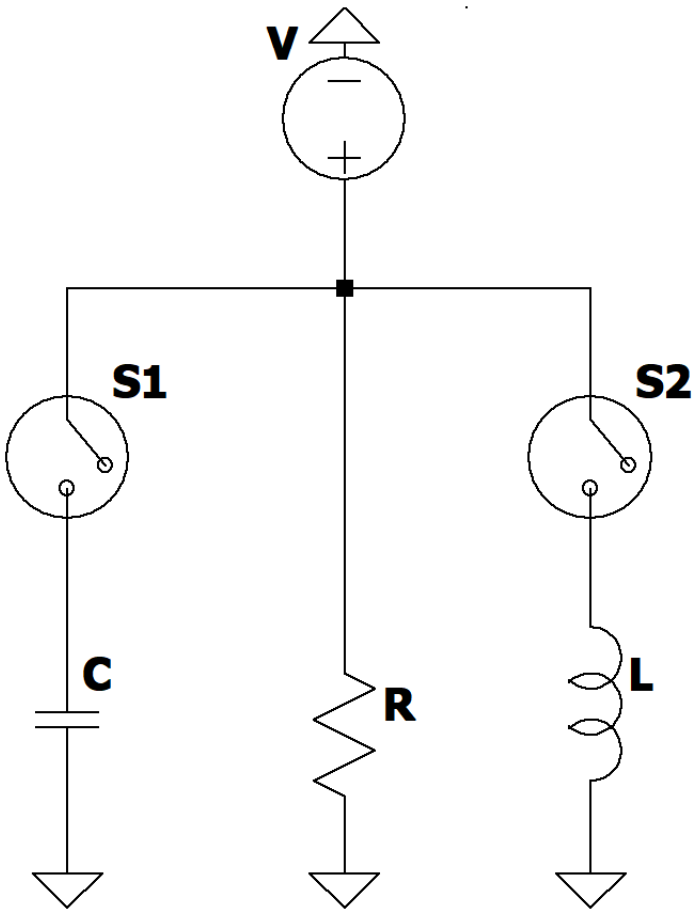

Figure 2.48: Ideal switching RL-RC impedance. The user is free to choose the phase between [-90°, 0°] by activating the RC load or between [0°, 90°] by activating the RL load.

This allows us to simulate a parallel switched RC - RL impedance with the following characteristics :

RC impedance

- R ∈ [1, 100 kΩ]
- C ∈ [20 pF, 20 nF]
- f ∈ [0 Hz, 5.7 kHz] (for the highest capacitor value).
- 0V < V_{in} < 5V

RL impedance

- R ∈ [1, 100 kΩ]
- L ∈ [1, 100H]
- f ∈ [159 Hz, $+\infty$]

- 0V $< V_{in} <$ 5V

This switching RC-RL impedance will be implemented in hardware in the CSL laboratory using the LM324 op amps. The obtained results will be discussed in the next section.

2.5 Practical implementation of the analog RLC impedance in the CSL lab

This section is dedicated to the practical implementation of the RLC impedance. The op amps used are the LM324[12] (provided by the CSL). This component consists of four independent operational amplifiers (two for the capacitor simulator and two for the inductor simulator). There are characterised by :

1. Gain Bandwidth Product : 1.3 MHz

2. CMRR : 80 dB

3. Max dual supply voltage : +/- 16 V

4. Typical Slew rate : 0.4 V/us (slow compared to the AD744 described in the previous section)

5. Open loop voltage gain : 100 dB

6. Max output current : 70 mA (for load of 2 kΩ) and 40 mA DC

7. Max output voltage : 13 V (for load of 2 kΩ)

The objective of this section is to compare the simulated results on LT Spice with those obtained from the real hardware implementation. The different values of the capacitor compared are : 2nF, 20 nF. On the other hand, the inductor values compared are 100 mH and 1 H.

2.5.1 Equivalent capacitor

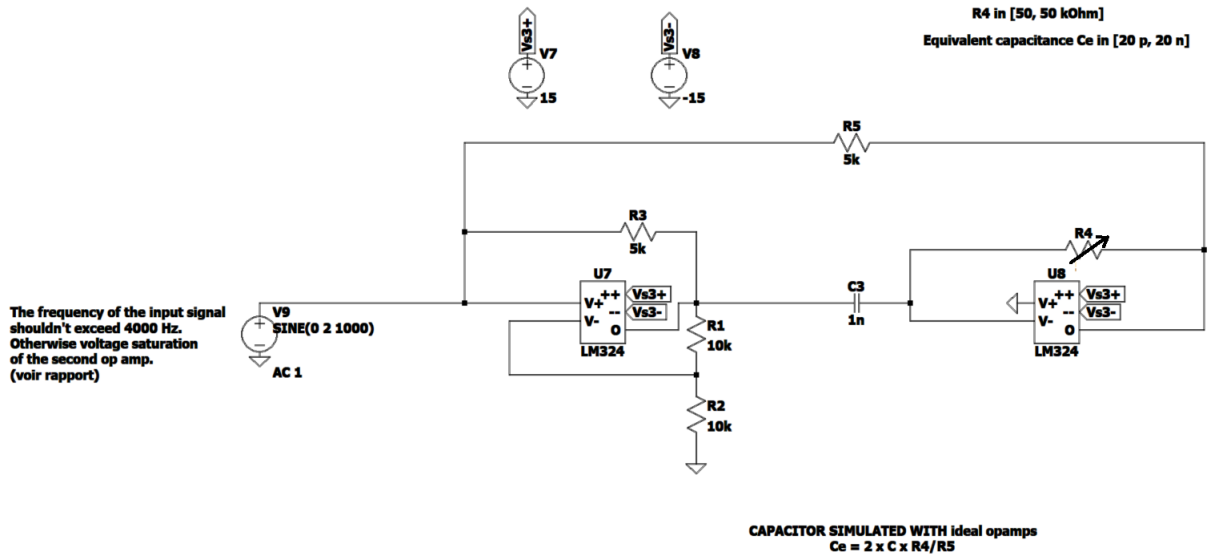

Figure 2.49: Circuit that simulates an ideal capacitor using the LM324 op amp.

The value of the capacitor can be adjusted using the potentiometer R_4. The frequency of the input signal shouldn't exceed 4000 Hz in order to prevent from any voltage saturation. The allowed capacitance values are between [20 pF, 20 nF]. Increasing it too much will lead to a voltage saturation as already shown in previous sections.

2.5.1.1 2 nF capacitor

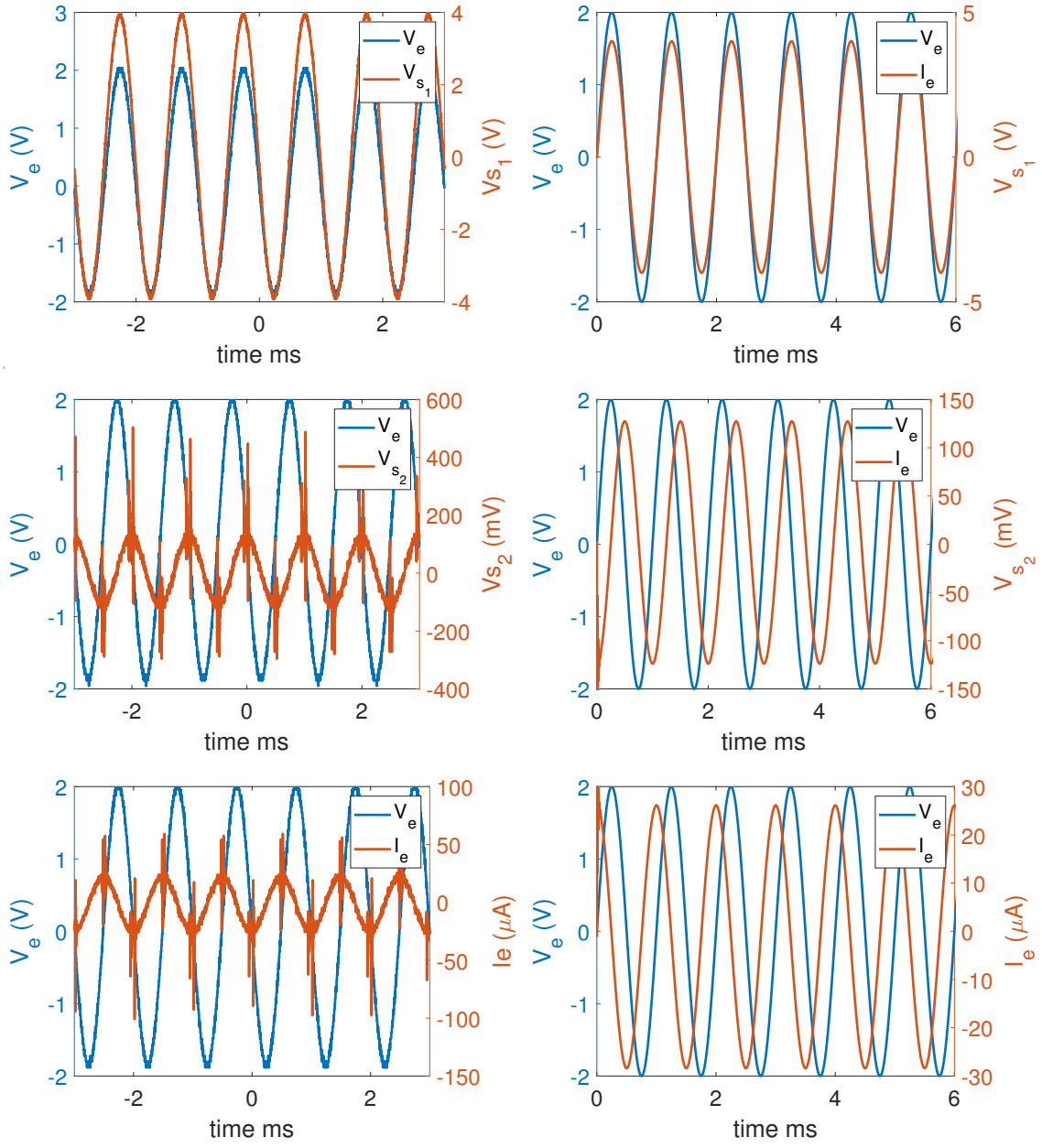

Figure 2.50: Capacitor simulated : 2 nF. These plots compare the characteristics of the hardware implementation (on the left-hand side) and the spice simulation (on the right-hand-side) in terms of the output voltage (V_{s_1}) of the first op amp, the output voltage (V_{s_2}) of the second op amp and the output current of the source generator (I_e).

Concerning the output voltage of the fist op amp (N.I.C circuit), the results obtained theoretically (confirmed by the LT spice simulation) match perfectly with the hardware implementation.

As demonstrated in subsection (2.2.3.4) the amplitude of the output voltage V_{s_1} should

be equal to :

$$|\hat{V}_{s_1}| = |\hat{V}_e|(1 + \frac{R_2}{R_1}) = 4 \text{ V}$$

Similarly, V_{s_2} should be equal to :

$$|\hat{V}_{s_2}| = |\hat{V}_e|(1 + \frac{R_2}{R_1})wCR_4 = 125 \text{ mV}$$

The fundamental frequency of the output voltage V_{s_2} is a sinus of amplitude 125 mV. But the signal is affected by high-frequency noise. The THD (total harmonic distortion) is 0.22 % and the SNR is 8.48 dB (quite low). The response at the output of the op amp will unfortunately affect the output current of the generator (I_e).

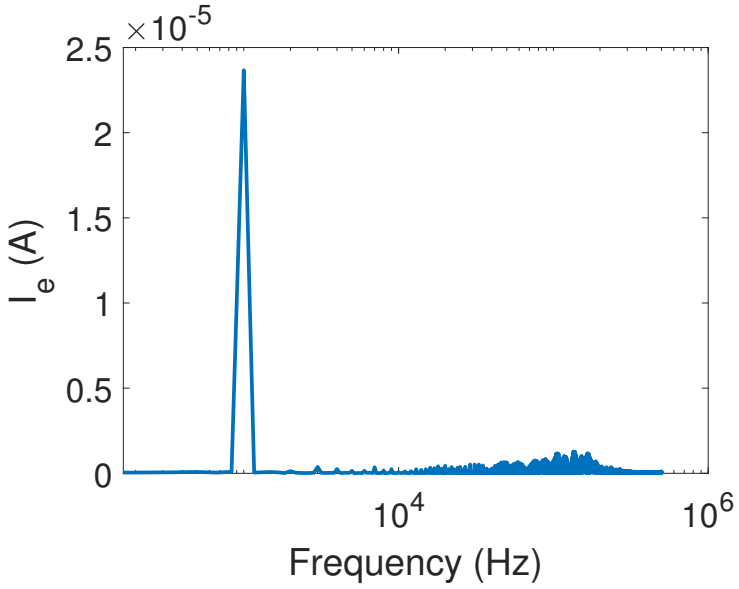

Figure 2.51: FFT of the output current (I_e) from the hardware implementation.

As can be seen from the above figure, the main component of the Fourier transform is at 1 kHz. This one is polluted by high frequency noise (above 10 kHz). The low SNR is due to the small CMRR (60 dB at 1 kHz). Furthermore, the LM324 is not a precision op amp (it's a kind of "general-purpose op amp"). The phase shift between the output current $\hat{I}_e$ and the input voltage $\hat{V}_e$ is 90 °. This comforts our motivation to build a "pure" capacitor.

2.5.1.2 20 nF capacitor

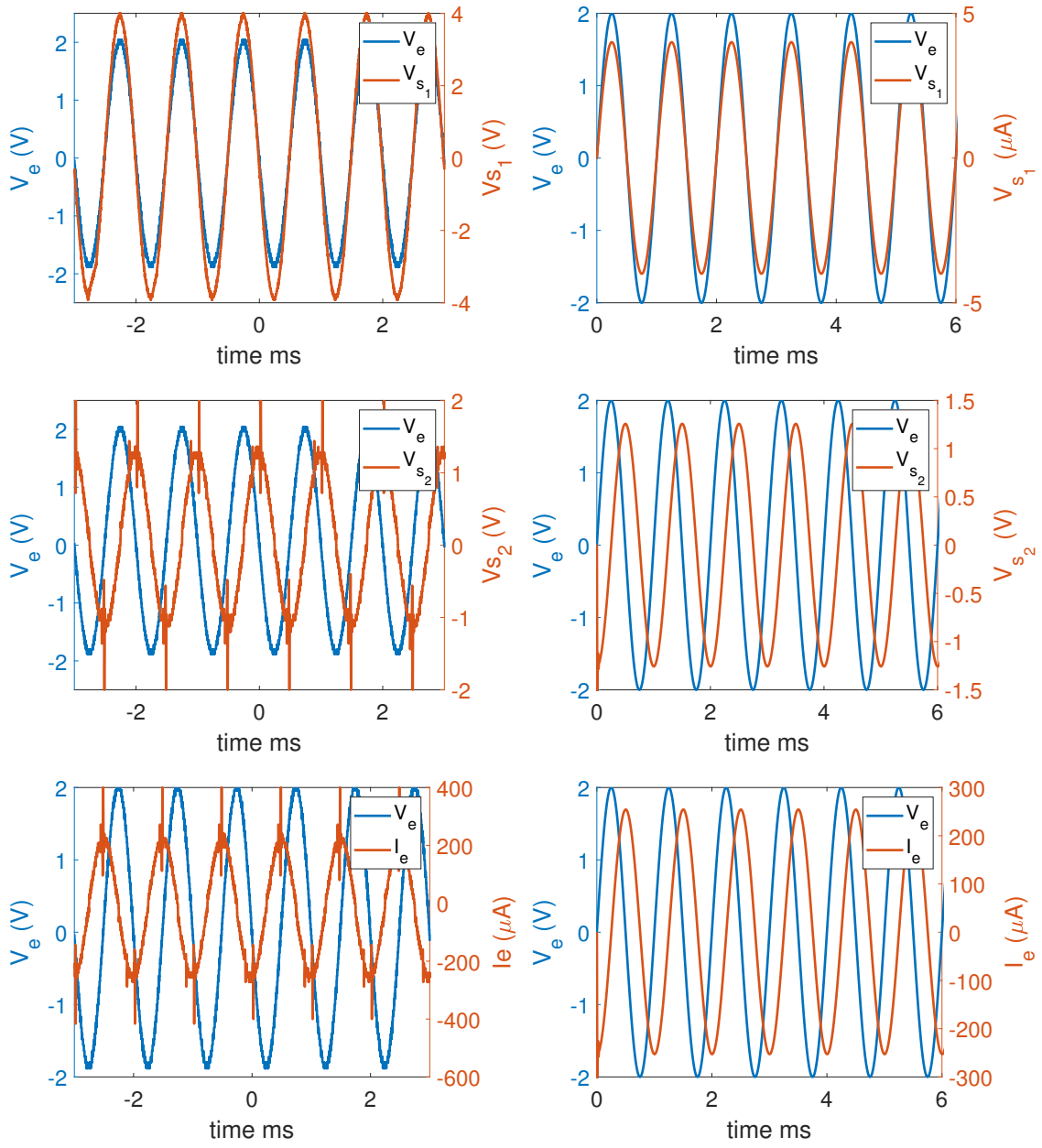

Figure 2.52: Capacitor simulated : 20 nF at 1000 Hz. These plots compare the characteristics of the hardware implementation (on the left hand side) and the spice simulation (on the right-hand side) in terms of the output voltage (V_{s_1}) of the first op amp, the output voltage (V_{s_2}) of the second op amp and the output current of the source generator (I_e).

For the 20 nF simulated capacitor, the obtained results from the hardware implementation are still polluted by high frequency noise. The main component of the signal is at 1000 Hz and matches well the simulated results on LT spice. The values can be verified

theoretically as described in section (2.2.3.4). It can be noticed that there is a phase shift of 90°between the output current $\hat{I}_e$ and input voltage ($\hat{V}_e$).

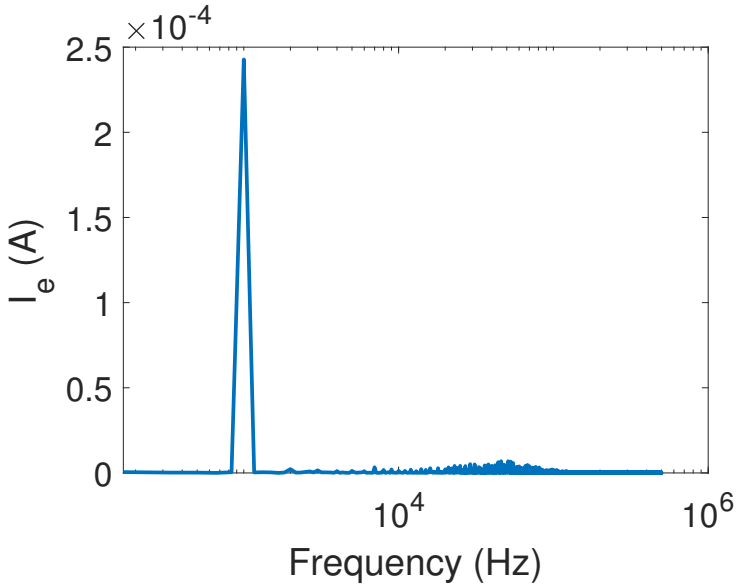

Figure 2.53: FFT of the output current (I_e) from the hardware implementation.

2.5.1.3 Frequency analysis

Let's study the frequency behaviour (small signal AC analysis) of this circuit for different equivalent capacitor valuee.

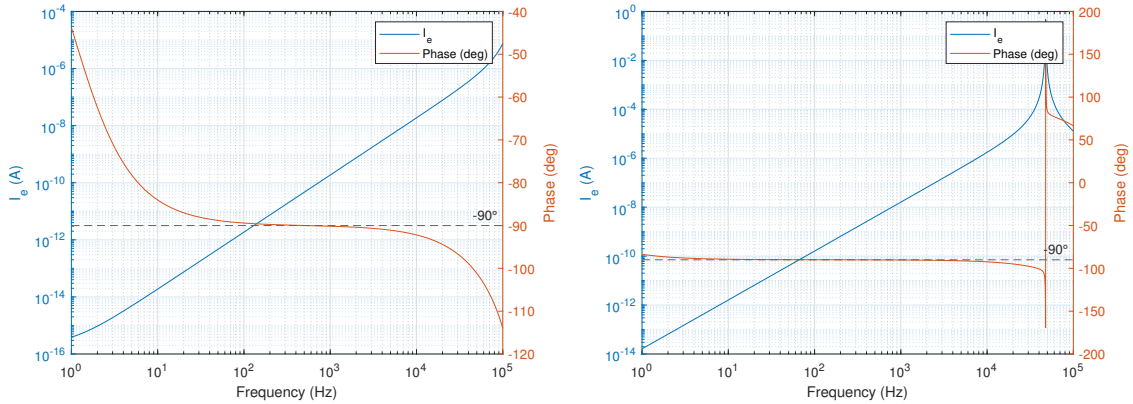

Figure 2.54: Frequency response of the equivalent capacitor circuit (with LM324 op amps) for different capacitor values : 2 nF (left figure), 20 nF (right figure). Small signal analysis with amplitude 1 Volt.

The two main following criteria are used in order to assess the performance of the equivalent capacitor circuit :

1. The bandwidth frequency for which the phase is near -90°"called the 90-degree-bandwidth". In this region, the phase of the input voltage $\hat{V}_e$ is phase shifted to -90°with respect to the output current $\hat{I}_e$. The equivalent is ideal.

2. The output current I_e should increase linearly with the frequency with slope (wC).

As can be seen from the above figure, the output current increases linearly with frequency specially in the 90-degree-bandwidth. Furthermore, this bandwidth becomes larger if the equivalent capacitor if the equivalent capacitor is higher.

2.5.2 Equivalent inductor

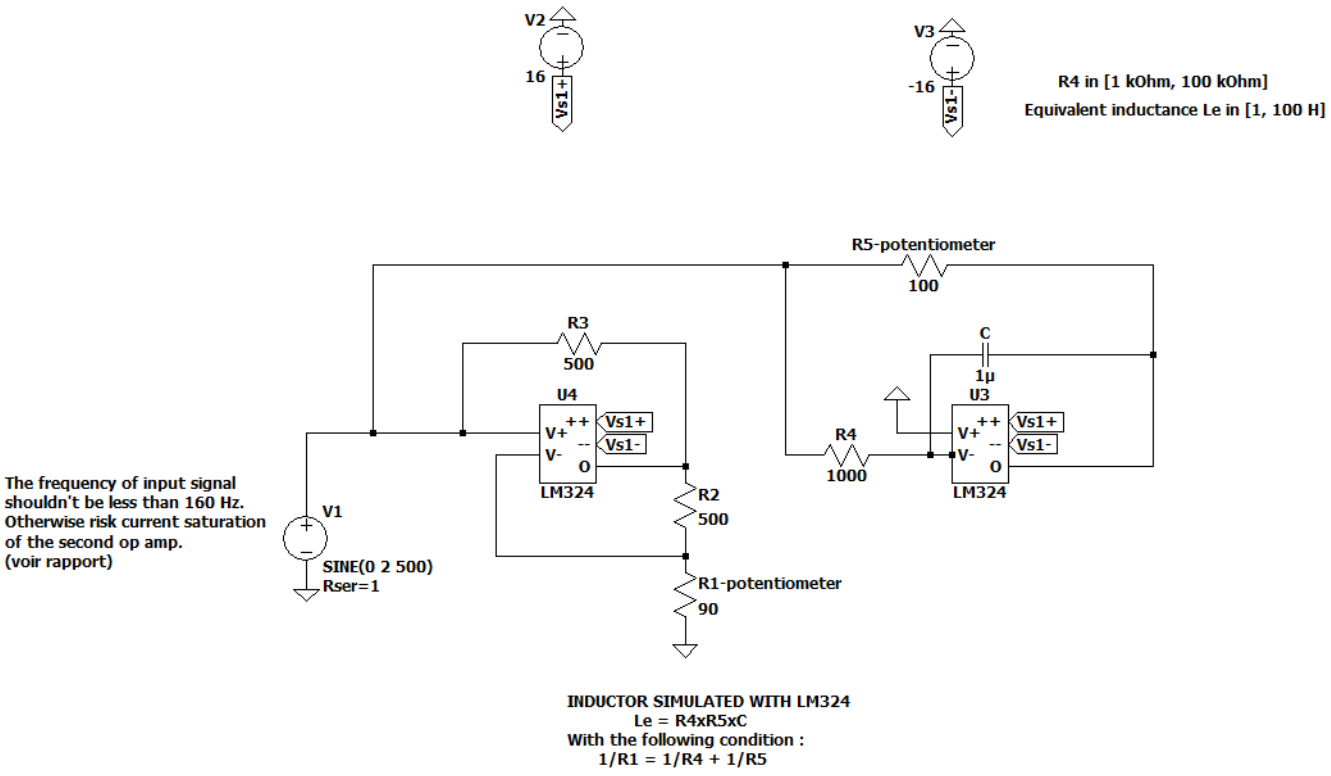

Figure 2.55: Circuit that simulates an ideal inductor using the LM324 op amp.

The value of the equivalent inductor can be adjusted using the potentiometer R_5. The frequency of the input signal shouldn't be less than 160 Hz in order to prevent from any current saturation. The potentiometer R_1 allows cancelling the parallel resistor in

order to get an ideal inductor. The allowed inductor values are between [1 H, 100 mH]. Decreasing it too much will lead to a current saturation (for small frequencies). The input signal frequency is set to 500 Hz by default in order to study its behaviour.

2.5.2.1 100 mH inductor

In order to get an 100 mH equivalent inductor, the potentiometer R_5 is set to 100 Ω. The potentiometer of the N.I.C R_1 is adjusted to 90 Ω to cancel the parasitic parallel resistor.

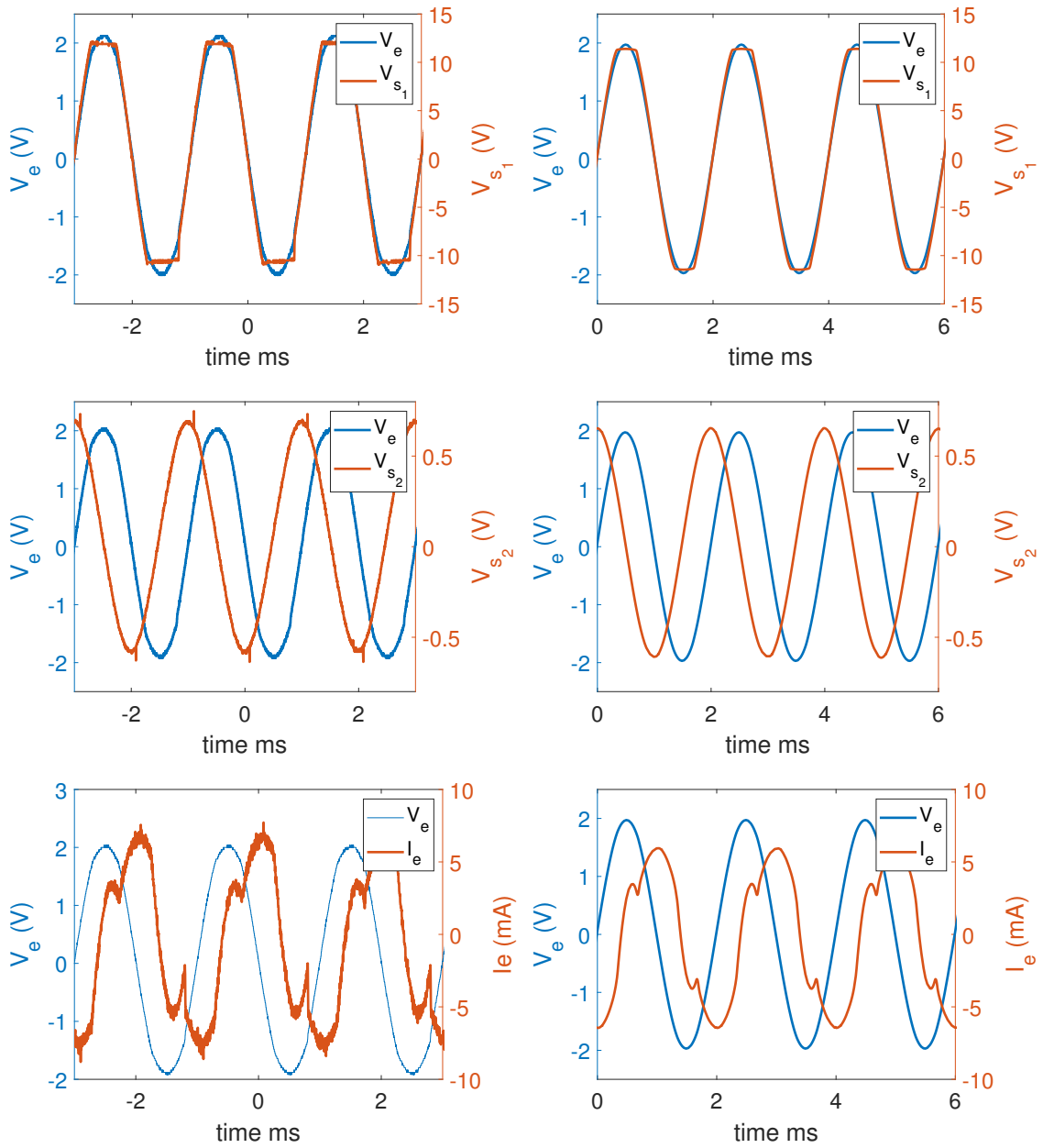

Figure 2.56: Inductor simulated : 100 mH. These plots compare the characteristics of the hardware implementation (on the left hand side) and the spice simulation (on the right-hand side) in terms of the output voltage (V_{s_1}) of the first op amp, the output voltage (V_{s_2}) of the second op amp and the output current of the source generator (I_e).

Since the value of the chosen inductor is below its minimum (1 H), the first op amp (N.I.C circuit) saturates at +/- 11 V. It's important to notice that the LM324 is not a rail-to-rail op amp and then saturates far below the power supply voltage (+/-16 V).

If the op amp was ideal, the output voltage Vs_1 should be equal to (see section 3.2.1.4) :

$$|\hat{V}_{s_1}| = |\hat{V}_e|(1 + \frac{R_2}{R_1}) = 13.1 \text{ V}$$

One can suggests that this issue can be solved by reducing the value of the resistor R_2 (and hence R_3 since they should be equal as described in section 3.3.1). Choosing R_2(i.e R_3) to 100 Ω will lead to an amplitude output voltage $|\hat{V}_{s_1}| = 4$ V. This way, we make sure that the first op amp associated to the N.I.C won't saturate. Unfortunately, a current saturation occurs instead. The output current $\hat{I}_{s_2}$ is equal to:

$$\hat{I}_{s_2} = \frac{\hat{V}_{s_1}}{R_1}(1 + \frac{R_2}{R_3}) = 44.4 \text{ mA}$$

On the other hand, the output voltage $\hat{V}_{s_2}$ of the second op amp matches well with the simulated results. It has been shown (section 3.3.1.4) mathematically that :

$$|\hat{V}_{s_2}| = \frac{|\hat{V}_e|}{wCR_4} = 636 \text{ mV}$$

Since the first op amp saturates, the output current of the generator $\hat{I}_e$ is distorted. The fundamental frequency remains at 500 Hz. It can also be noticed that the main fourier's component of the output current is phase shifted by -90°.

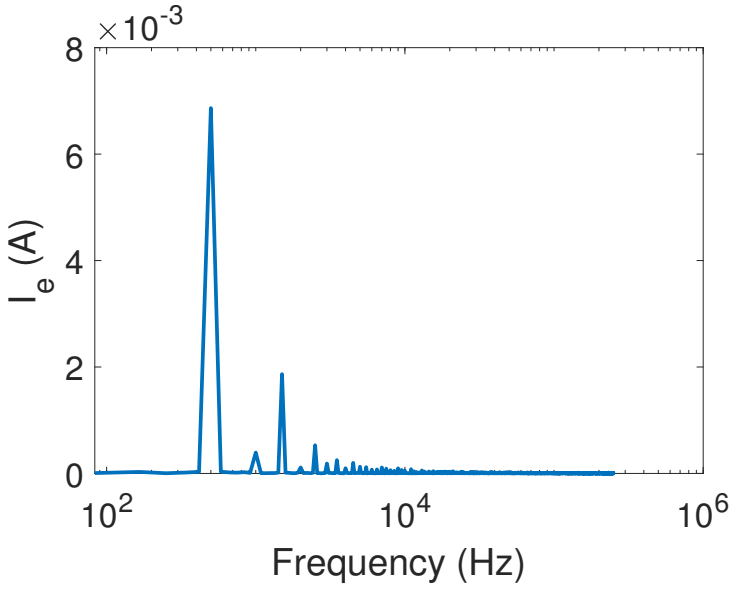

Figure 2.57: FFT of the output current (I_e) from the hardware implementation.

As can be seen from the above figure, the fft of the output current I_e shows that the main

component remains at 500 Hz. There are some harmonics due to the saturation of the first op amp. The total harmonic distortion (THD) is 8.6%. The SNR is low : 21.59 dB.

2.5.2.2 1 H inductor

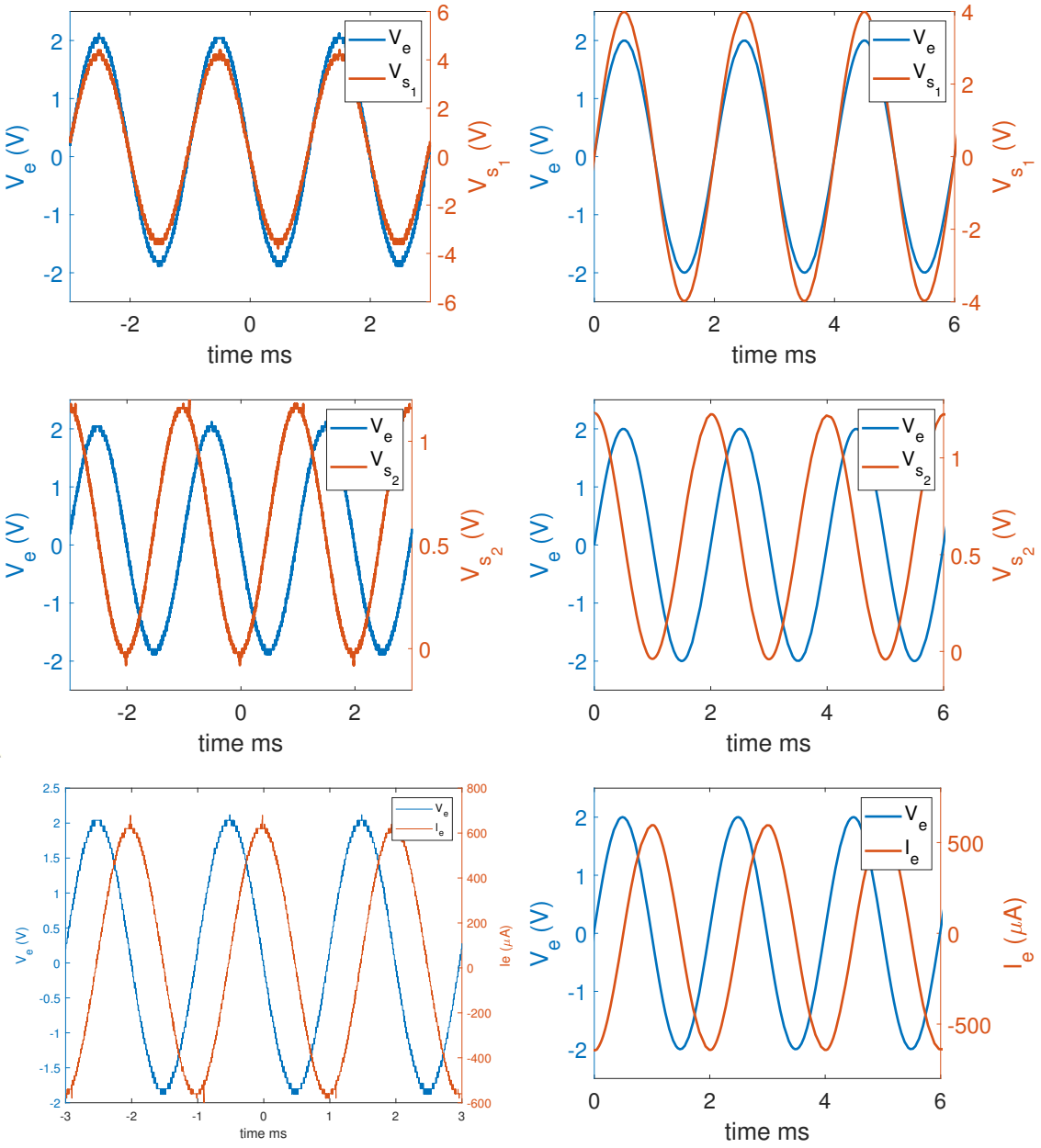

Figure 2.58: Inductor simulated : 1 H. These plots compare the characteristics of the hardware implementation (on the left hand side) and the spice simulation (on the right-hand side) in terms of the output voltage (V_{s_1}) of the first op amp, the output voltage (V_{s_2}) of the second op amp and the output current of the source generator (I_e).

For the 1 H simulated inductor, the obtained results from the hardware implementation matches well with the simulated results on LTspice. The values can be verified theoretically as described in section (2.2.3.4). It can be clearly seen from the above figure that there is a phase shift of -90°between the output current $\hat{I}_e$ and the input voltage $\hat{V}_e$.

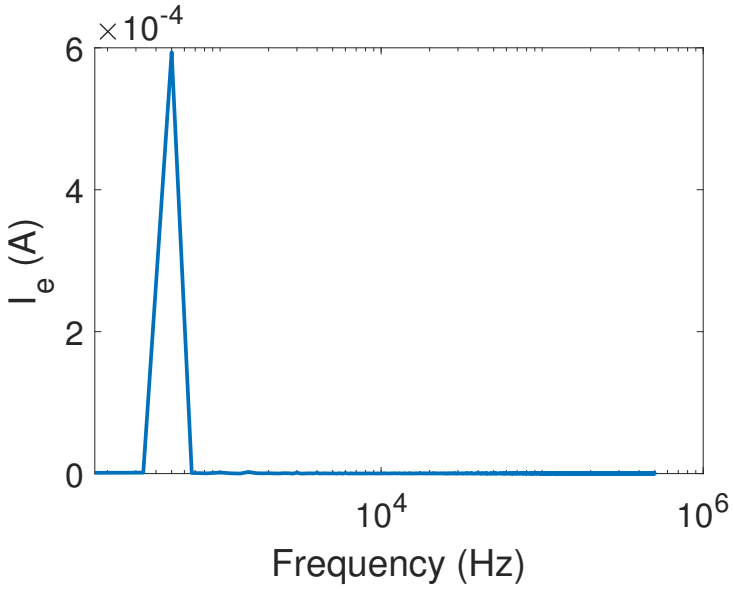

Figure 2.59: FFT of the output current (I_e) from the hardware implementation.

The fourier's transform of the output current I_e shows a single nice fringe located at 500 Hz. There's no harmonic distortion and the signal is not polluted by high frequency noise.

2.5.2.3 Frequency analysis

Let's now study the frequency behaviour (small signal AC analysis) of the gyrator for different equivalent inductor values. The LM324's are still used for the gyrator implementation.

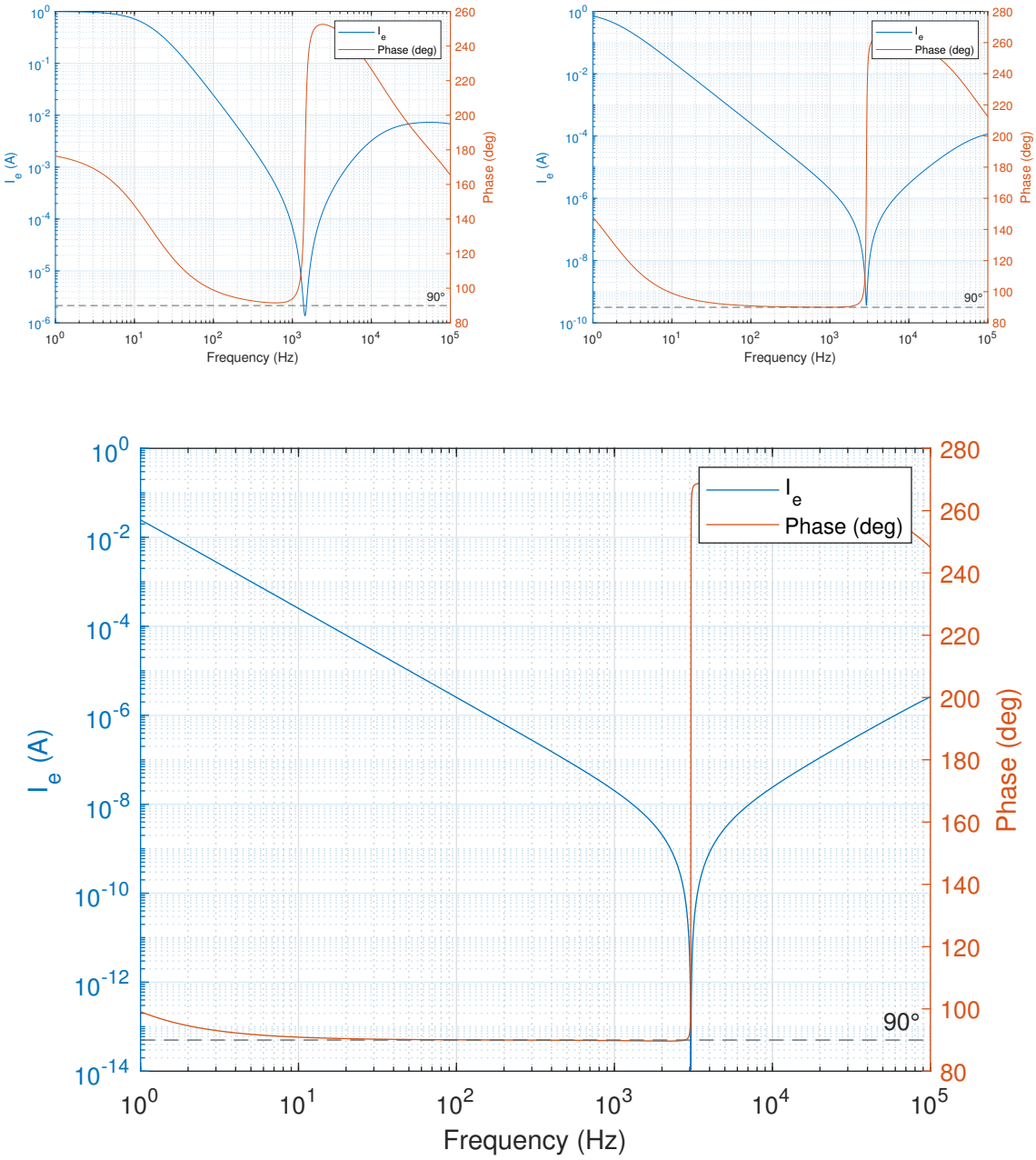

Figure 2.60: Frequency response of the gyrator circuit (with LM324 op amps) for different inductor values : 10 mH (top left figure), 100 mH (top right figure) and 1 H (last figure). Small signal analysis with amplitude 1 Volt.

As mentioned previously for the equivalent capacitor circuit (subsubsection 5.1.3) One of the main criteria to evaluate the quality of the gyrator circuit is the phase shift between the output current $\hat{I}_e$ and the input voltage $\hat{V}_e$. A phase shift of 90°means that an ideal inductor is simulated by the circuit. This means that the N.I.C plays well its role and no current/voltage saturation occurs at the output of the LM324 op amps. The bandwidth frequency for which the phase is near 90°"called the 90-degree-bandwidth" is a good

indicator of the equivalent inductor perfomance. The larger the 90-degree-bandwidth is, the more accurate it is (no distortion or saturation). It can clearly be seen from the above figures that this bandwidth increases with the chosen inductor values. Furthermore, there exists a cut off frequency where the circuit becomes unstable (2 kHz).

The second criterion is the linear (log-scale : warning !) behaviour of the output current with respect to the frequency. For a perfect inductor, the output current I_e should decrease with slope 1/(wL) for given input voltage. This is confirmed by the above figures. I_e decreases linearly (log scale) wrt to frequency inside the 90-degree-bandwith.

2.5.3 Discussion

As mentioned in previous sections, the main limitations are the maximum output voltage/output current. They reduce the frequency range for which the equivalent capacitor/inductor behaves like real components. For the capacitor, a voltage or current saturation occurs if the frequency of the input signal is too high. On the other hand, if the frequency of the input signal is too low (DC), the ideal inductor behaves as a short-circuit. This leads to a voltage/current saturation.

Using power op amps may improve the 90-degree-bandwidth since they tolerate high output voltage and output current. The OPA548[13] is a good choice here because it allows a maximum output current of 5 amps (the output is internally buffered) and the voltage saturation occurs above 30 V.

As with any op amp circuit, the performance of gyrators at high frequencies depends on the op amp bandwidth. So a gyrated inductor/capacitor will stop looking like an inductor/capacitor at frequencies greater than a few percent of the op amp bandwidth (see [14] for more information).The simulation results in figure 5.12 show the behaviour of the gyrated inductor wrt to frequency. Roughly speaking, the nearly perfect inductor (at low frequencies) becomes a capacitor at high frequencies with a resonance in between. This may appear quite nasty but notice that the inductor has an impressive high quality

factor of about 6000 at 1 kHz (for $L_{equiv} = 1$ Henry) assuming that the ESR of the gyrated inductor is 1 Ω. So the third criterion that should be considered is the gain bandwidth product (GBW). A higher GBW means greater loop gain, and higher loop gain means lower error (gain, phase, distortion). Since the op amps of the N.I.C and the gyrator are used with the negative feedback, the open loop should stay high enough to make sure that the inverting and the non-inverting input stay at same potential : $V^+ = V^-$.

3 Digital implementation

3.1 Schematic overview

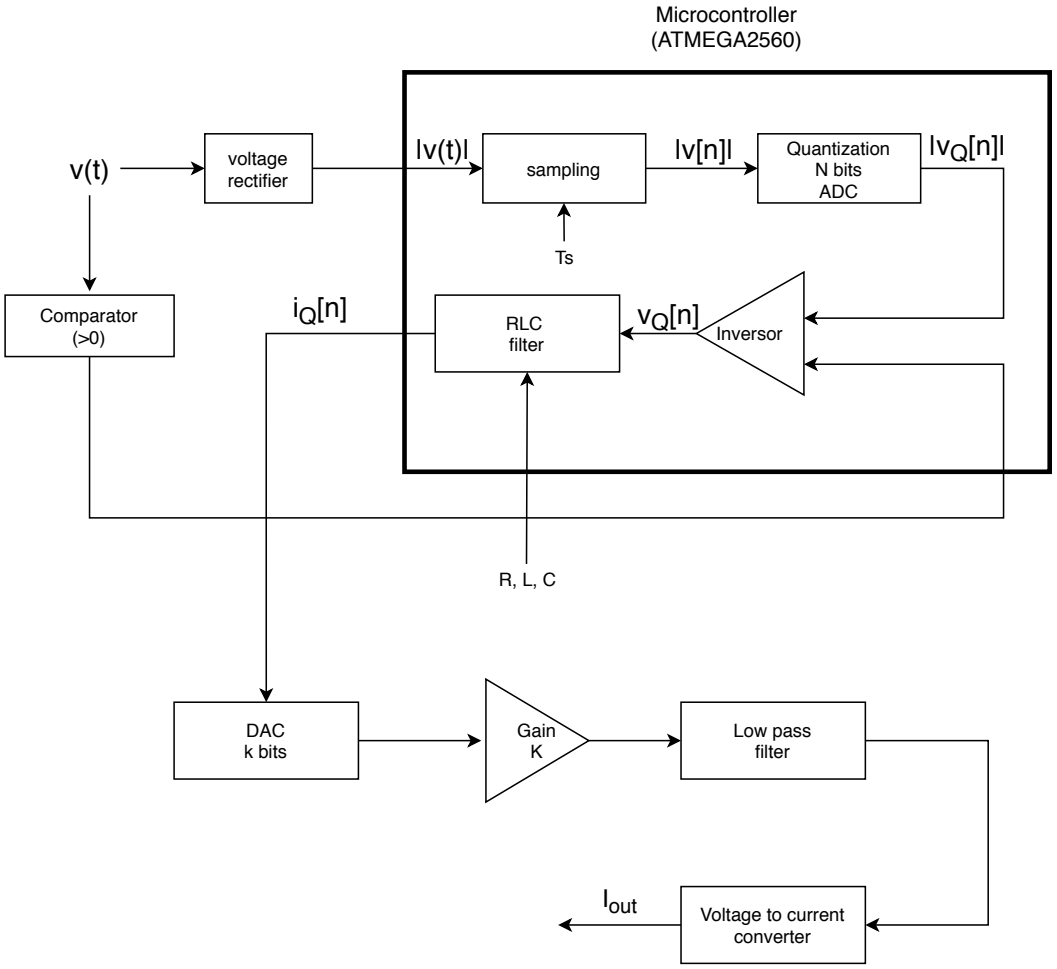

Figure 3.1: Schematic of the digital implementation of the RLC impedance.

Let's consider a continuous input voltage $v(t)$. This one has to be sampled at sampling period T_s by the microcontroller. Assuming that the microcontroller cannot afford to take as input a negative voltage (most general case), the input voltage has to be rectified. The sign of $v(t)$ has to be adjusted digitally inside the microcontroller after the analog-to-digital converter. The voltage is quantized with N bits and fed into a RLC filter. The digital implementation of the RLC filter will be described in the next section. The RLC filter outputs an "image" of the quantized output current $i_Q[n]$.The output current is then converted to analog through the DAC [15] (k bits accuracy). It's important to notice that the output current is in fact represented by a voltage (which is an image of the output current). Finally, the voltage reflecting the output current is converted into current by a voltage-to-current converter after some gain adjusting and low-pass filtering to remove the noise quantization. The output current is injected into the generator and the loop is closed.

Here's more a simplified schema of the digital implementation :

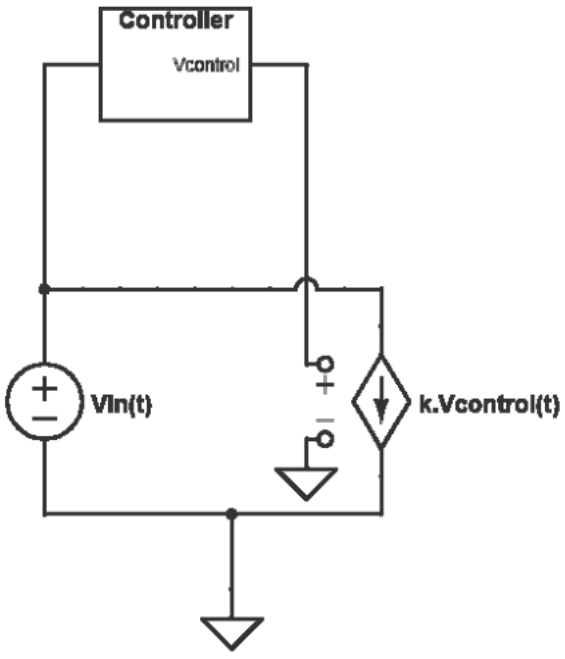

Figure 3.2: Simplified representation of the digital implementation. The current injected to the generator is controlled by the microcontroller. It's proportional to the current that would flow into an inductor or capacitor.

By correctly adjusting $V_{control}(t)$ according to the value of the inductor or capacitor, it's

possible to simulate an inductive/capacitive load across the generator. Let's study in the next section how $V_{control}(t)$ can be derived from digital filtering.

3.2 Digital RLC filter

Let's first focus on the most important part : the digital implementation of the RLC filter. As performed for the analog impedance, the parallel RLC impedance will be first simulated.

3.2.1 Time domain

3.2.1.1 Continuous time domain

Let's consider a continuous input voltage $v(t)$, the current across the resistor can be computed by the Ohm's Law :

$$\hat{i}_R = \frac{v(t)}{R} \tag{i}$$

The current across the capacitor is :

$$i_C(t) = C\frac{dv(t)}{dt} \tag{ii}$$

The current across the inductor is such that :

$$\frac{di_L(t)}{dt} = \frac{v(t)}{L} \tag{iii}$$

For a RC parallel load, the total current can be expressed as

$$i_{RC}(t) = i_R(t) + i_C(t) = \frac{v(t)}{R} + C\frac{dv(t)}{dt} \tag{iv}$$

For the RL parallel load, the total current can be expressed as :

$$i_{RL}(t) = i_R(t) + i_L(t) = \frac{v(t)}{R} + \frac{1}{L}\int_{t_0}^{t} v(t)dt \tag{v}$$

3.2.1.2 Discrete time domain

Let $v[n]$ be the sampled input voltage at sampling period T_s. The current across the resistor is

$$i_R[n] = \frac{v[n]}{R} \tag{vi}$$

The derivative term associated to the capacitor can be descretized this way :

$$i_C[n] = \frac{C}{T_s}(v[n] - v[n-1]) \tag{vii}$$

The integrative term associated to the inductor can also be decretized :

$$i_L[n] = i_L[n-1] + \frac{1}{L}T_s v[n-1] \tag{viii}$$

For a RC parallel load, the total current can be expressed as

$$i_{RC}[n] = i_R[n] + i_C[n] = \frac{v[n]}{R} + \frac{C}{T_s}(v[n] - v[n-1]) \tag{ix}$$

Similarly, for a RL parallel load, the total current can be expressed as :

$$i_{RL}[n] = i_R[n] + i_L[n] = \frac{v[n]}{R} + i_L[n-1] + \frac{1}{L}T_s v[n-1] \tag{x}$$

The two expressions (ix), (x) will be implemented in the microcontroller.

Let's plot the discrete output current generated by our digital implementation and compare with the continuous output current. [2]

[2]LtSpice is used for the simulations. See [16] for discrete implementations on LtSpice.

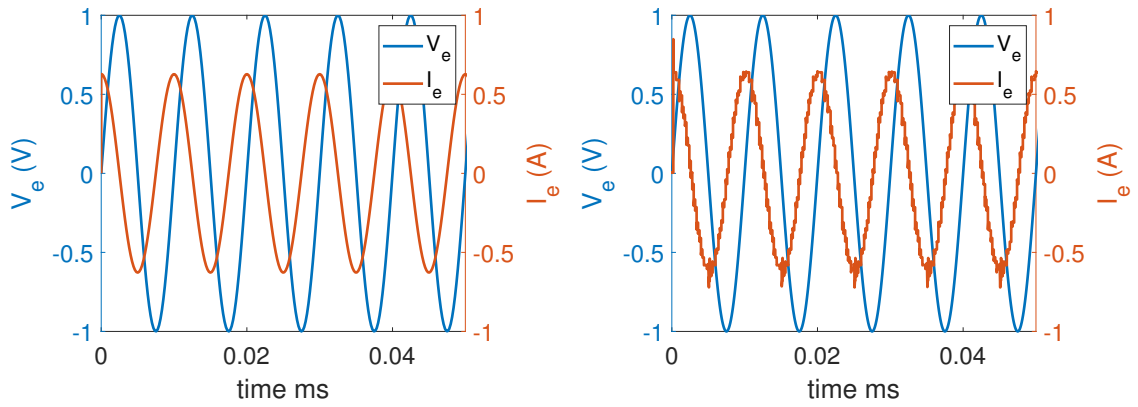

Figure 3.3: Simulated capacitor : 1 mF. Left plot : continuous output current. Right plot : discrete output current generated by the microcontroller at sampling frequency 5000 Hz. The input voltage is a 100 Hz sine wave.

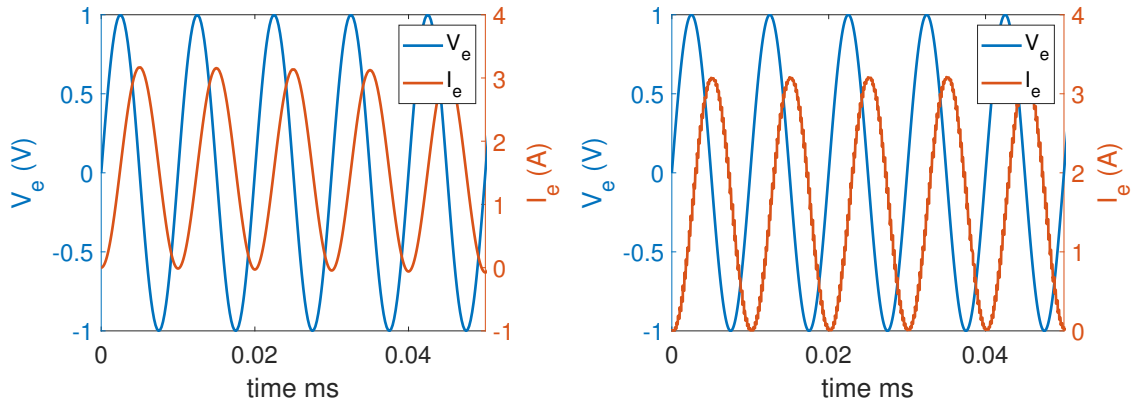

Figure 3.4: Simulated inductor : 1 mH. Left plot : continuous output current. Right plot : discrete output current generated by the microcontroller at sampling frequency 5000 Hz. The input voltage is a 100 Hz sine wave.

cfr LTspice digital circuit named "DIGITAL RLC FILTER" to test the performance of the digital implementation. Change various parameters such as the value of the capacitor, inductor, sampling frequency, frequency of the input signal, ... And see what happens ...

The discrete output current that has been generated by the microcontroller can be low-filtered in order to remove the noise due to the sampling frequency. However, it may add an additional phase shift to the output current and the 90 degree phase shift between the input voltage and output current may not be satisfied. A low pass filter should be considered if the magnitude of the output current only matters. Otherwise, the cutoff frequency should be set far away from the fundamental frequency of the input voltage. This will be discussed in the frequency domain section.

3.2.2 Frequency domain

The transfer function between the input voltage and the output current can be computed for the two domains :

- Laplace domain : associated to the continuous time.

- Z-domain : associated to the discrete time. More useful here since a discrete filter will be implemented.

A frequency analysis can be performed by studying the transfer functions.

3.2.2.1 Laplace Transform

The current across the resistor is :

$$\hat{I}_R(s) = \frac{\hat{V}(s)}{R} \tag{xi}$$

The current across the capacitor is :

$$\hat{I}_C(s) = sC\hat{V}(s) \tag{xii}$$

The current across the inductor is :

$$\hat{I}_L(s) = \frac{V(s)}{sL} \tag{xiii}$$

For the RC parallel load, the output current in the Laplace domain can be expressed as :

$$\hat{I}_{RC}(s) = \frac{\hat{V}(s)}{R} + sC\hat{V}(s) \tag{xiv}$$

For a RL load :

$$\hat{I}_{RL}(s) = \frac{\hat{V}(s)}{R} + \frac{V(s)}{sL} \tag{xv}$$

The transfer function $H_{RC}(s)$ between the input voltage and the output current can be deduced :

$$\hat{H}_{RC}(s) = \frac{hatI_{RC}(s)}{V(s)} = \frac{1}{R} + sC \tag{xvi}$$

Similarly for the inductive load, the transfer function H_{RL} can be expressed as :

$$\hat{H}_{RL}(s) = \frac{\hat{I}_{RL}(s)}{V(s)} = \frac{1}{R} + \frac{1}{sL} \tag{xvii}$$

The continuous transfer functions $\hat{H}_{RL}$ and $\hat{H}_{RC}$ are the equivalent admittance (in Siemens).

Let's study the transfer functions in the Laplace domain and Z-domain. The RL and RC filters will be analysed in the frequency domain using the bode plot.

RC filter

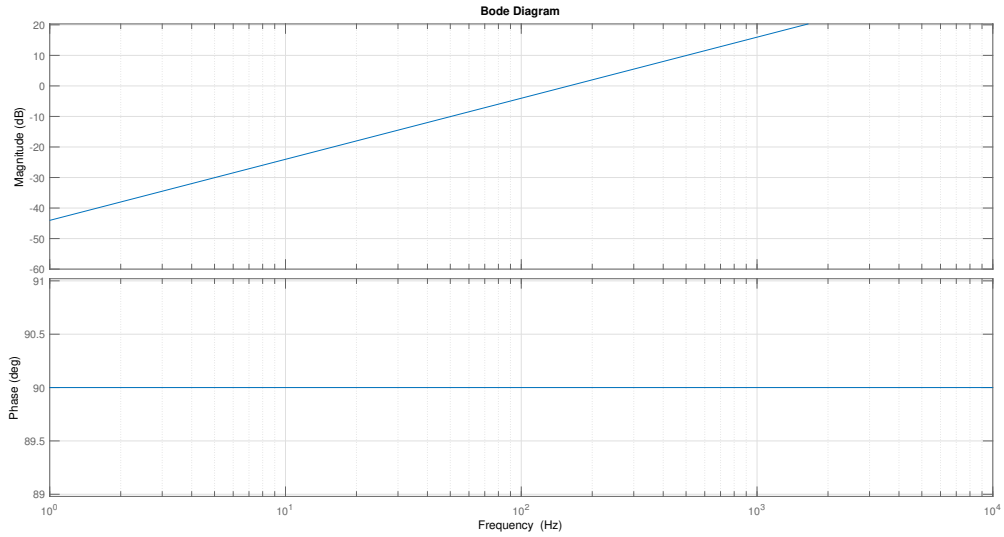

Figure 3.5: Bode plot of a continuous ideal capacitor (1 mF).

The above figure shows the main characteristics of continuous RC filter :

- Increasing linear gain (log-scale) with frequency.

- Constant 90° phase shift.

It will be shown in the next subsection that those two characteristics will be altered in the digital domain. The main limitation will be the sampling frequency.

RL filter

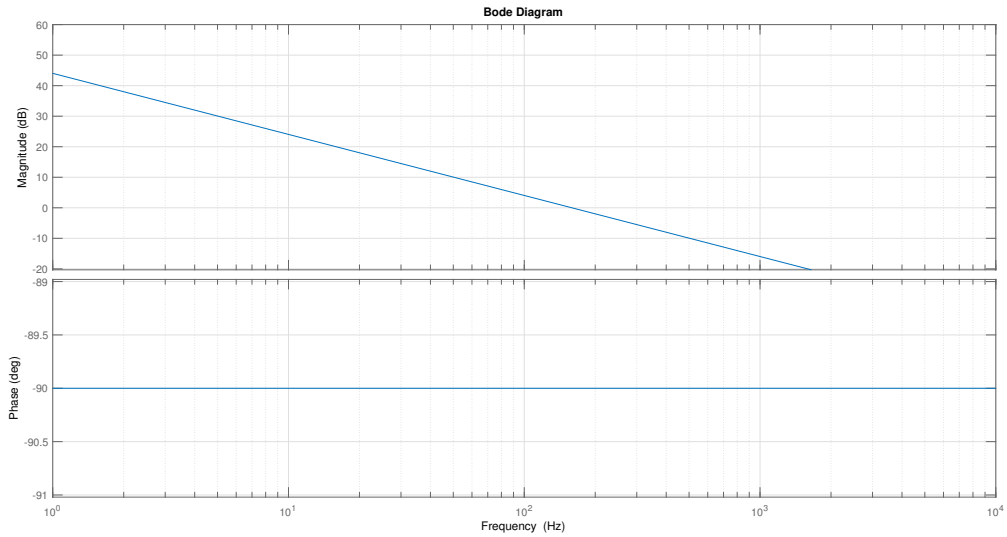

Figure 3.6: Bode plot of a continuous ideal inductor (1 mH).

As performed for the RC filter, it can be deduced that :

- Decreasing linear gain with frequency (log-scale).
- Constant -90° phase-shift.

3.2.2.2 Z-transform

The current across the resistor is :

$$\hat{I}_R(z) = \frac{\hat{V}(z)}{R} \tag{xviii}$$

The current across the capacitor is :

$$\hat{I}_C(z) = \frac{C}{T_s}\hat{V}(z)(1 - z^{-1}) \tag{xix}$$

The current across the inductor is :

$$\hat{I}_L(z) = \frac{1}{L} T_s \frac{V(z) z^{-1}}{1 - z^{-1}} \tag{xx}$$

For the RC parallel load, the output current in the Laplace domain can be expressed as :

$$\hat{I}_{RC}(z) = \frac{\hat{V}(z)}{R} + \frac{C}{T_s} \hat{V}(z)(1 - z^{-1}) \tag{xxi}$$

For the RL load :

$$\hat{I}_{RL}(z) = \frac{\hat{V}(z)}{R} + \frac{1}{L} T_s \frac{V(z) z^{-1}}{1 - z^{-1}} \tag{xxii}$$

The transfer function $H_{RC}(z)$ between the input voltage and the output current can be deduced :

$$\hat{H}_{RC}(z) = \frac{\hat{I}_{RC}(z)}{V(z)} = \frac{1}{R} + \frac{C}{T_s}(1 - z^{-1}) \tag{xxiii}$$

Similarly for the inductive load, the transfer function $H_{RL}(z)$ can be expressed as :

$$\hat{H}_{RL}(z) = \frac{\hat{I}_{RL}(z)}{V(z)} = \frac{1}{R} + \frac{1}{L} T_s \frac{z^{-1}}{1 - z^{-1}} \tag{xxiv}$$

Let's study the two transfer functions $\hat{H}_{RL}$ and $\hat{H}_{RC}$ in the Z-Domain. Let's take R close to ∞ in order to simulate an ideal capacitor and inductor. Since the signal is discrete in the Z-Domain, the transfer function depend on the sampling frequency. The analog to digital conversion is limited to 10 kSamples per second (100 µs to perform one conversion). The digital filter requires 77 µs for each sampling period. This limits the maximum sampling frequency to 5600 Hz.

Digital RC filter

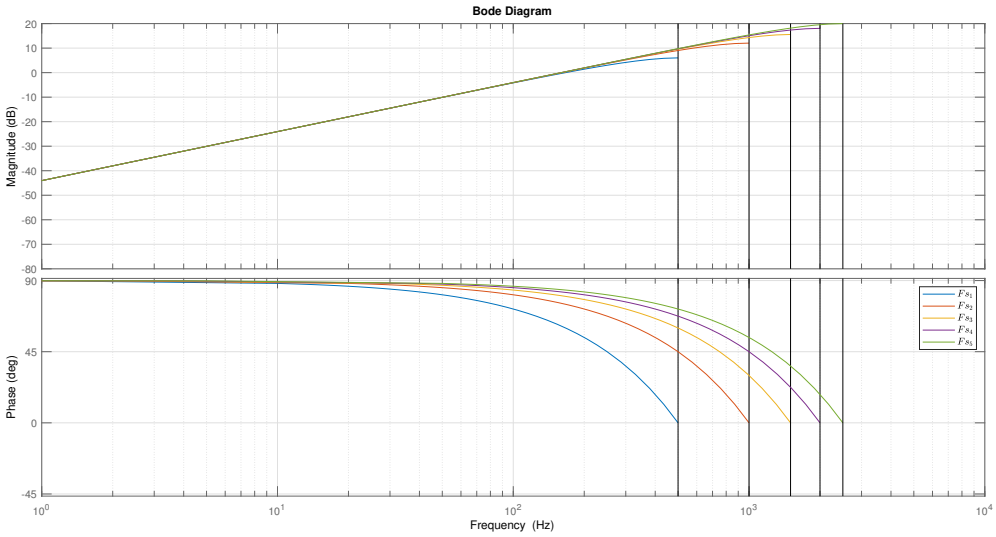

Figure 3.7: Bode plot of the digital ideal capacitor (1 mF) transfer function for different sampling frequency : Fs_1, Fs_2,Fs_3, Fs_4 and Fs_5 respectively equal to 1, 2, 3, 4 and 5 kHz.

As can be seen from the above figure, the behaviour of our digital filter is strongly linked to the sampling frequency. The greater the sampling frequency, the larger can be the input signal bandwidth. The filter stops being stable at half the sampling frequency. Furthermore, the magnitude response and the phase doesn't behave the same way at half the sampling frequency. In fact, the phase decreases much faster than the gain which limits the available frequency bandwidth of the input signal if we want to simulate an ideal capacitor with 90° phase-shift. On the other hand, the gain is less impacted by the frequency. This one stays nearly linear until the Nyquist frequency.

As said previously, since the maximum sampling frequency is limited to 5600 Hz, the maximum frequency of the input signal shouldn't exceed half the sampling frequency. The available frequency bandwidth is limited depending on the degree of importance is granted to the phase shift. If one considers that the 90° phase shift doesn't matter, the available frequency bandwidth can be extended until the Nyquist frequency since the gain remains linear. This amounts to simulate an ideal capacitor in terms of gain without taking care of the 90°phase shift. Furthermore, an analog low pass filter can be designed

in order to keep only the signal below the sampling frequency without being afraid of the consequence on the phase-shift. On the other hand, if both gain and phase-shift matter, the available frequency bandwidth becomes narrower (for a given sampling frequency). And using a low-pass filter becomes less attractive due to the potential phase-shift it can produce.

Digital RL filter

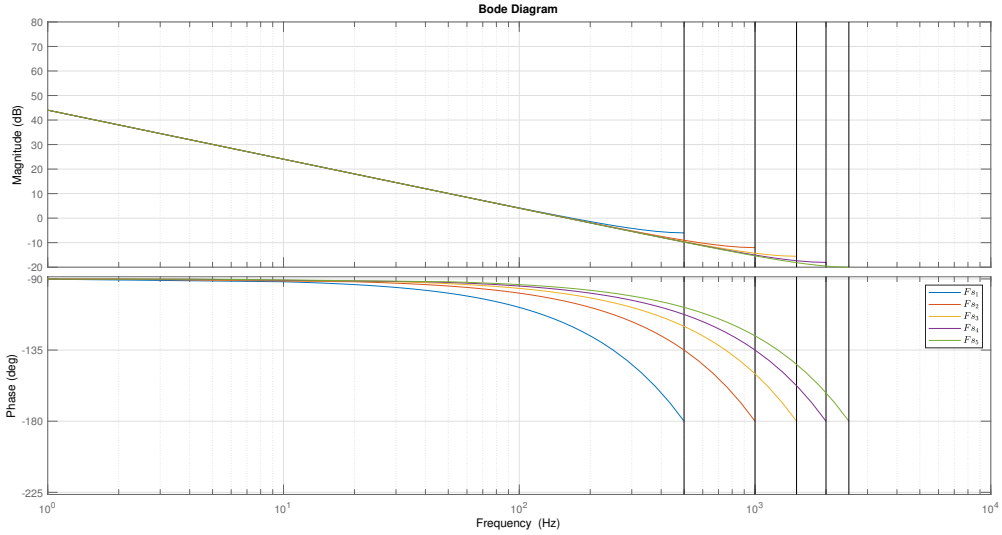

Figure 3.8: Bode plot of the digital ideal inductor (1mH) transfer function for different sampling frequency : Fs_1, Fs_2,Fs_3, Fs_4 and Fs_5 respectively equal to 1, 2, 3, 4 and 5 kHz.

For the discrete RL filter in the frequency domain : same comment as above (about the discrete RC filter). Two main differences can be noticed :

1. The gain now decreases linearly (Log-scale!) with respect to the frequency until the Nyquist frequency. Logical since the filter is inductive.
2. The phase-shift is now -90° between current and voltage (far away from the Nyquist frequency).

3.3 Hardware part of the digital implementation

A digital implementation doesn't always refer to a fully digital circuit. Some high stage analog circuits are used in order to relieve the microcontroller from power operations. Several analog stage have to be implemented in order to manage properly data gathering from the microcontroller. The digital implementation must be embedded in a hardware part. Let's enumerate the four analog blocks :

1. Voltage rectifier : rectifies the input voltage because the microcontroller can't afford a negative voltage.
2. Comparator : if the input voltage becomes negative, alert the microcontroller !
3. Voltage follower : it's high input impedance reliefs the microcontroller from dissipating power.
4. Howland current source : converts controlled voltage to current.

3.3.1 Voltage rectifier

Since the microcontroller (ATMEGA2560[17]) isn't able to deal with a negative voltage. The input signal has to be rectified. Using a full bridge rectified here is a bad idea because the signal can be aliased due to the voltage drop across the diodes. Instead, a precision full-wave rectifier[18] made of op amps can be used. The output signal is not distorted but must stay between the positive power supply.

Here's the circuit :

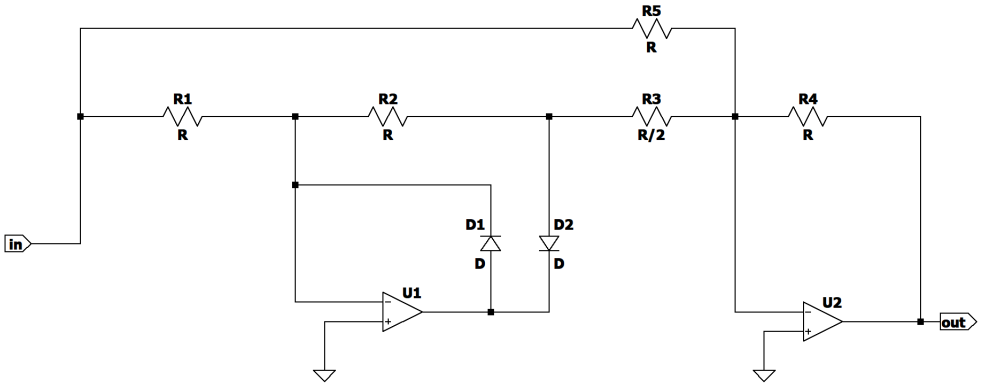

Figure 3.9: Full-wave precision rectifier.

3.3.2 Comparator

The comparator plays a role in alerting the microcontroller when the voltage drops below zero. It consists of an op amp supplied between positive voltage and ground. The op amp works in unstable mode. It outputs a logical "1" only when the input voltage is below 0.

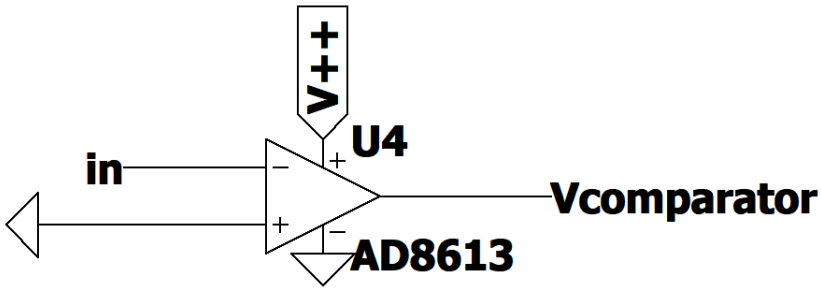

Figure 3.10: Comparator that outputs logical "1" if the input voltage is below the reference : 0 V.

3.3.3 Voltage follower

The microcontroller outputs a voltage v_{dac} that has to be converted into current by the voltage to current converter. It's important to prevent the microcontroller from drawing

too much current. Thus a voltage follower is useful here. It's characterised by its high input impedance (Mega Ω).

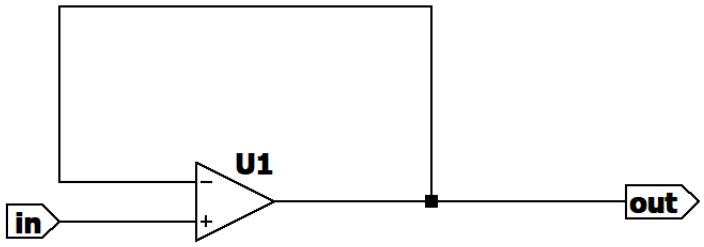

Figure 3.11: Voltage follower.

3.3.4 Howland current source

The objective now is to convert the controlled voltage into current. This current will be injected to the voltage generator in order to simulate a fictive inductive/capacitive load.

A famous circuit made of ap amps called **Howland current source**[19] allows converting a voltage source to a current source into a load. This circuit plays the most important role of the embedded circuit. It consists of an operational amplifier and a balanced resistor bridge to maintain the constant current value through the load even if the value of load resistance changes.

The idea is to keep the same principle of the Howland source by replacing the output load by the generator :

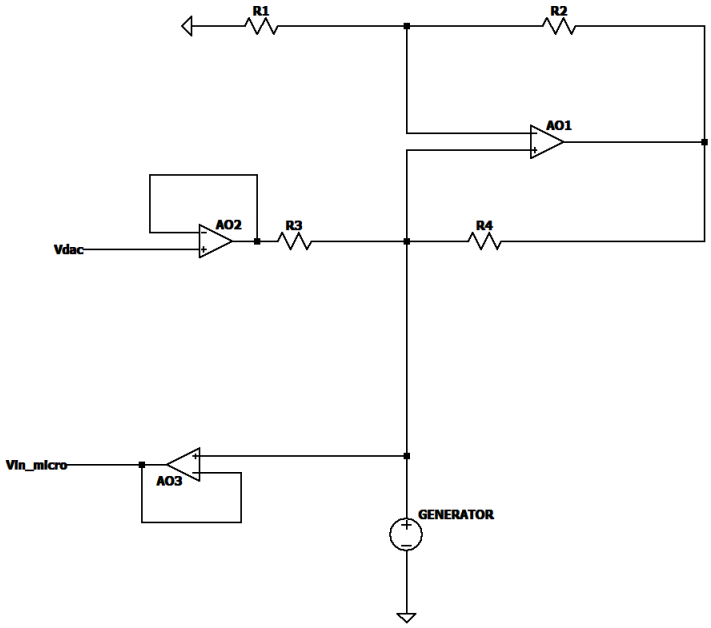

Figure 3.12: Howland current source. Vdac is the controlled voltage at the output of the DAC. It has to be converted into current. $V_{\text{in\_micro}}$ is the voltage of the generator which goes into the input pin of the microcontroller (before the voltage rectifier).

Assuming that the op amp is ideal and V^{+}=V^{-}, it can be deduced that :

$$V^{-} = V_o \frac{R_1}{R_1 + R_2} = V^{+} = V_{GENERATOR}$$

It can be deduced from the Ohm low that the current through R_3 and R_4 are :

$$I_{R_3} = \frac{V_{dac} - V_{GENERATOR}}{R_3}$$

$$I_{R_4} = \frac{V_o - V_{GENERATOR}}{R_4}$$

The current that goes through the generator can be computed using Kirchhoff's current law :

$$\begin{aligned} I_{GENERATOR} = I_{R_3} + I_{R_4} &= \frac{V_{dac} - V_{GENERATOR}}{R_3} + \frac{V_o - V_{GENERATOR}}{R_4} \\ &= \frac{V_{dac} - V_{GENERATOR}}{R_3} + \frac{V_{GENERATOR}(R_1 + R_2)}{R_1 R_4} - \frac{V_{GENERATOR}}{R_4} \\ &= \frac{V_{dac} - V_{GENERATOR}}{R_3} + \frac{V_{GENERATOR} R_2}{R_1 R_4} \\ &= \frac{V_{dac}}{R_3} + V_{GENERATOR}(-\frac{1}{R_3} + \frac{R_2}{R_1 R_4}) \end{aligned}$$

If the following condition is satisfied :

$$\frac{1}{R_3} = \frac{R_2}{R_1 R_4} \tag{xxv}$$

The current through the generator depends only on the voltage at the output of the DAC becomes:

$$I_{GENERATOR} = \frac{V_{dac}}{R_3} \tag{xxvi}$$

Let's now determine the values of the resistors R_1, R_2, R_3, R_4 such as the Howland and the voltage follower op amp never saturates. The OPA548 is a good choice here because it is internally buffered which allows 5 A peak. Furthermore, it can be supplied between +/-30 V.

The output current of the Howland op amp is :

$$I_{OH} = V_{GENERATOR}(\frac{1}{R_4} + \frac{1}{R_3}) \leq 5 \text{ A} \tag{xxvii}$$

And its output voltage :

$$V_{OH} = V_{GENERATOR}(1 + \frac{R_2}{R_1}) \leq 25 \text{ V} \tag{xxviii}$$

The output current of the voltage follower op amp is :

$$I_{R_4} = \frac{V_{DAC} - V_{GENERATOR}}{R_3} \leq 5 \text{ A} \tag{xxix}$$

If the peak generator never exceeds 5 V, it can be derived from (xxvii) :

$$\frac{1}{R_4} + \frac{1}{R_3} \leq 1 \tag{xxx}$$

In order to avoid any current saturation of the voltage follower op amp (xxvii) :

$$V_{DAC} - V_{GENERATOR} \leq 5R_3$$

$$|V_{DAC} - V_{GENERATOR}|_{max} \leq 5R_3$$

$$R_3 \geq 1 \tag{xxxi}$$

From (xxviii), the following condition should always be satisfied to avoid a voltage saturation :

$$\frac{R_2}{R_4} \leq 4$$

Let's choose $R_3 = 1\ \Omega$ in order to get a perfect mirror of the current at the output of the DAC :

$$\frac{V_{DAC}}{1\Omega} = I_{GENERATOR}$$

But this is a bad idea since the condition (xxviii) will never be satisfied. This may lead to a current saturation of the Howland op amp.

Let's take instead $R_3 = 2\Omega$ and $R_4 = 2\Omega$. The condition (xxx) is thus satisfied.

In order to always satisfy the condition (xxv) :

$$R_2 = R_3 = 10k\Omega \tag{xxxii}$$

The resistor R_3 plays the role of a conversion gain between voltage and current.If it is chosen equal to 2 Ω, there will always be a factor 2 between the V_{DAC} and $I_{GENERATOR}$. V_{DAC} can be multiplied by 2 thanks to voltage amplifier and always get :

$$I_{GENERATOR} = \frac{2V_{DAC}}{2} = \frac{V_{DAC}}{1\Omega}$$

The input voltage V_{DAC} is now a perfect image of the generator current $I_{GENERATOR}$.

3.3.5 Assembling digital and analog implementation

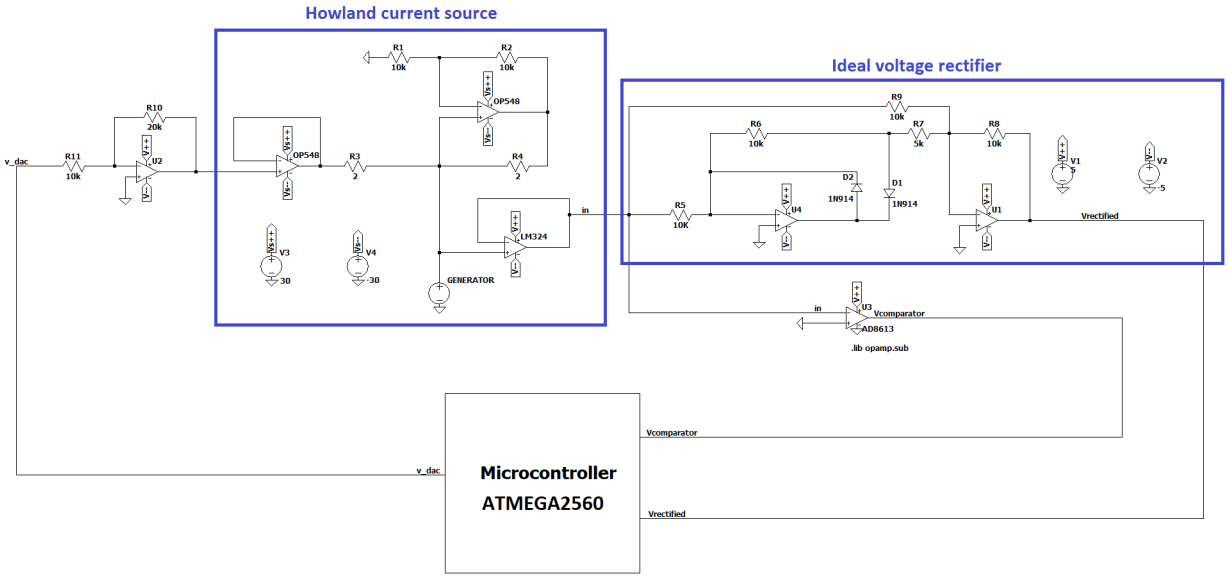

Figure 3.13: Final embedded digital implementation. See Appendix A for a landscape format of the digital implementation.

The output current that goes through the generator is a perfect image of the controlled voltage v_dac. See LTspice file named : "DIGITAL RLC FILTER.asc". This circuit is simulated for a 1 mF capacitor. The frequency of the input signal is $F_{sig} = 100$ Hz. The sampling frequency $F_s = 5000$ Hz. The ADC is 10 bits accuracy and the DAC is 12 bits accuracy.

4 Discussion

Two kinds of implementations have been suggested with their pros and cons. The analog RLC impedance makes use of a gyrated capacitor and a gyrated inductor connected in parallel with a potentiometer. The filtering process is performed analogically by contrast

to the digital RLC impedance. The main limitations for both implementations remain the maximum output current and the maximum output voltage that can afford the op amps. Those two parameters depends on the RMS value of the input voltage and its frequency. They also affect the available range of inductance/capacitance values. This is why the choice of a good op amp is important here. The op amps should be buffered in order to allow a much larger output current. But the voltage saturation is unavoidable at higher frequencies. The gyrators in the analog implementation and the Howland current in the digital implementation make use of the negative feedback. Therefore the gain bandwidth product of the op amp matters if we want to increase the 90-degree-bandwidth for the analog impedance. The digital impedance allows switching easily the configuration of the RLC impedance from parallel to series connection. Whereas most gyrators are ground referenced, they can only replace an inductor/capacitor that is returned to ground, but not a floating inductor making impossible a series connection. The maximum frequency of the input signal is limited by the sampling frequency of the microcontroller (Shannon-Nyquist theorem).

The available inductance and capacitance range can be compared for both implementations in the following table :

Equivalent Loads	**Analog impedance**				**Digital impedance**	
	Current limitations	Voltage limitations	Adjustments	Conditions	Current limitations	Adjustments
Le	$\lvert \mathrm{I}_{s_1} \rvert = \frac{\lvert \hat{V}_e \rvert}{R_1}\left(\frac{R_2}{R_3}+1\right) < I_{\mathrm{Lim}}$ $\lvert \mathrm{I}_{s_2} \rvert = \lvert V_e(\frac{2}{R_4}+\frac{1}{R_5}+\frac{1}{R_4 R_5 \hat{Y}}) \rvert < I_{\mathrm{Lim}}$	$\lvert \mathrm{V}_{s_1} \rvert = \lvert \hat{V}_e \rvert (1+\frac{R_2}{R_1}) < V_{\mathrm{sat}}$ $\lvert \mathrm{V}_{s_2} \rvert = \frac{\lvert \hat{V}_e \rvert}{\lvert \hat{Y} \rvert R_4} < V_{\mathrm{sat}}$	$L_e = R_4 R_5 C$	$\mathrm{R}_3 = \frac{R_2}{R_1}\frac{R_4 R_5}{R_4+R_5}$	$\frac{V_e}{2\pi f L_e} < I_{\mathrm{Lim}}$	on software
Ce	$\lvert \mathrm{I}_{s_1} \rvert = \lvert \hat{V}_e(\frac{R_2}{R_3 R_1}+(1+\frac{R_2}{R_1})\hat{Y}+\frac{1}{R_1}) \rvert < I_{\mathrm{Lim}}$ $\lvert \mathrm{I}_{s_2} \rvert = \lvert \hat{V}_e \rvert \left((1+\frac{R_2}{R_1})\hat{Y}(1+\frac{R_4}{R_5})+\frac{1}{R_5}\right) \rvert < I_{\mathrm{Lim}}$	$\lvert \mathrm{V}_{s_1} \rvert = \lvert \hat{V}_e \rvert (1+\frac{R_2}{R_1}) < V_{\mathrm{sat}}$ $\lvert \mathrm{V}_{s_2} \rvert = \lvert \hat{V}_e \rvert (1+\frac{R_2}{R_1}) \lvert \hat{Y} \rvert R_4 < V_{\mathrm{sat}}$	$\mathrm{C}_e = \frac{R_1+R_2}{R_1}\frac{R_4}{R_5}C$	$\mathrm{R}_5 = \frac{R_3 R_1}{R_2}$	$V_e 2\pi f C_e < I_{\mathrm{Lim}}$	on software

Table 4.1: Comparison between the analog/digital RLC impedance. The appendix A and B contains the final electric diagram of both implementations.

Let's fix the input voltage and the input frequency bandwidth discussed with Mr N. Martin (my internship supervisor) :

$$V_e \in [0, 5V]$$

$$f \in [0 \text{ Hz}, 1 \text{ kHz}]$$

For the analog impedance, the resistors of the equivalent inductor/capacitor R_1, R_2, R_3, R_4 and R_5 have been computed in order to maximize the range of inductance/capacitance values for the given range of input voltage and frequency.

Resitors	Gyrated inductor	Gyrated capacitor
R_1	variates	10 kΩ
R_2	500Ω	10 kΩ
R_3	500Ω	5 kΩ
R_4	1000Ω	variates, fixes C
R_5	variates, fixes L	5 kΩ

Table 4.1: Values of resistors for the gyrated inductor/capacitor.

If the power op amp OPA548 is used for both implementations, the following available capacitance/inductance range can be derived :

Available ranges		
Elements simulated	Digital impedance	Analog Impedance
C	[230 pF, 159 µF]	[4 pF, 0.15 µF]
L	[16 mH, 100 H]	[145 mH, 100 H]

Table 4.2: Comparisons of available inductance/capacitance ranges between analog/digital impedances.

As can be seen from the above table 4.2, the digital implementation offers more flexibility to the range of the inductance/capacitance values. Furthermore, as shown in table 4.1, it contains fewer constraints than the analog impedance. Concerning the analog implementation, the range of admissible capacitance/inductance values will strongly

depend on the values of the resistors around the op amp.

5 Conclusion

The goal of this thesis was to develop a programmable RLC impedance with adjustable resistor, capacitor and inductor. Two kinds of implementations have been suggested. First, the analog impedance whose inductance/capacitance values are adjusted using potentiometers. Second, the digital implementation whose inductance/capacitance values are fixed on software. Both implementations have their pros and cons.

The analog impedance is mainly limited by the maximum output voltage/current that can afford the op amps of the gyrated capacitor and inductor. The theoretical limits have been computed assuming an infinite open-loop gain with perfect negative feedback. Several spice simulations have been performed to analyze the performance of the gyrators using the precision op amp AD744. The gyrated capacitor and inductor have been implemented on a breadboard using the LM324 op amp. The output current of the generator has been compared with the simulated results on LTspice.

On the other hand, the main limitations of the digital implementation are the sampling frequency and the maximum output current of the Howland current source op amp. LTspice simulator has been used to assess the performance of the digital RLC filter for different inductance/capacitance values.

Finally, the commonalities and differences of the two implementations are discussed in the last chapter. The available inductance/capacitance ranges are compared for a fixed input voltage and frequency bandwidth.

6 Appendix

6.1 Appendix A

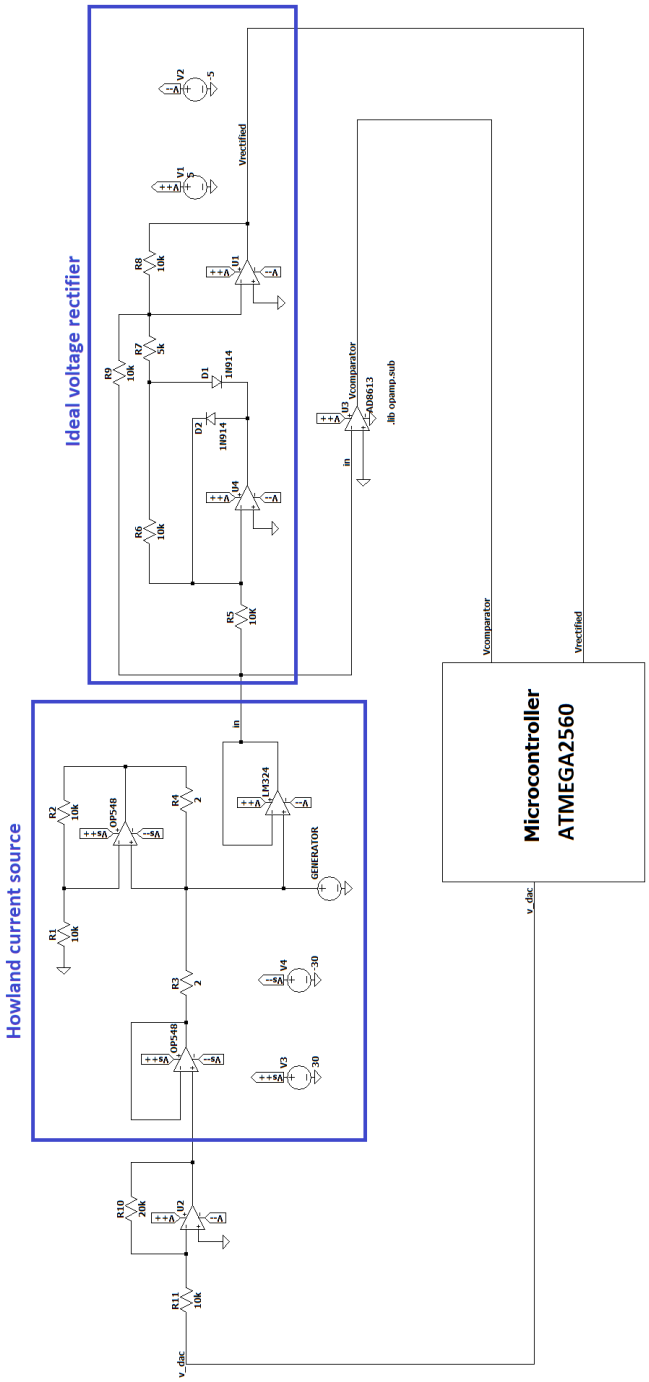

Figure 6.1: Final digital implementation of the programmable RLC impedance.

6.2 Appendix B

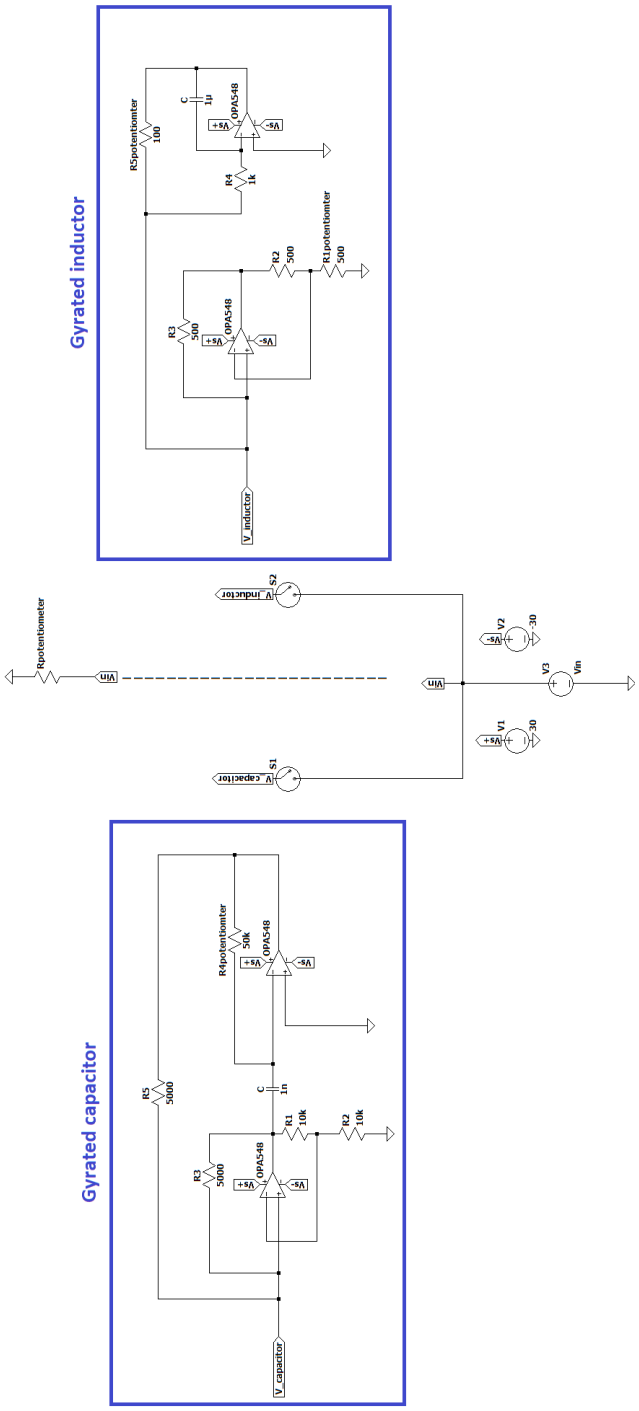

Figure 6.2: Final analog implementation of the programmable RLC impedance.

6.3 Appendix C

6.3.1 The Space Center of Liège

The main objective of the Centre Spatial de Liège[3] / Liège Space Center is to provide products and services of the highest quality and to the satisfaction of all its partners.

The Centre Spatial de Liège (CSL) is determined to maintain the certifications relating to its quality management system and to carry out its activities under controlled conditions in accordance with its certifications, national and international standards in force.

The overall objectives of the CSL are defined as follows[4]:

- Maintain a sustainable working environment;
- Satisfy the needs of its partners in technological innovation;
- Ensure the conformity of its products and services with applicable and contractually defined standards and requirements (Cost - Quality - Timeliness and more particularly in terms of "Design-to-Cost", "On-Time-Delivery", "OnQuality-Delivery");
- Continuously improve internal operating procedures in terms of risk management, skills management, reliability of project forecasts, protection of sensitive data, etc;
- Prepare for developments in the space industry in order to remain a key partner in space instrumentation and in the spatial data processing value chain;
- Measure the performance of its processes and actions taken to improve the effectiveness of its quality management system.

The CSL has many expertise :

1. **Optics & Imaging** : Design & Simulation, Calibration, Metrology, Remote Sensing, ...

[3]This small appendix is taken from [20].
[4]cited by Mr Michel BOGAERTS : Chief Executive Officier (ad interim).

2. **Space Environment** : Design Analysis, On ground Testing, Cleanliness and Cyogenic application
3. **COATING SURFACE TECHNOLOGIES** : Thin films and coatings, Ion & plasma processes, Micro nanostructures, Optical sensors, ...
4. **THERMAL & MECHANICAL ENGINEERING** : Thermal design & Analysis, Mechanical design, Mechanism design, Cryogenics, Material & processes
5. **ELECTRONIC ENGINEERING** : Space verification facilities development, Space scientific payloads development, Embedded systems engineering.
6. **QUALITY** : Quality & Risk Management, Product & Quality Assurance, National Surveillance Organisation.

This master thesis is part from electronic engineering sector. The CSL has an electronic lab[5] that supports the design and development of any embedded system. The electronic lab extensively supports the vacuum tests and the optical metrology by automating the vacuum test facilities, robotizing the optical metrology benches and designing and manufacturing stimulus Electrical Ground Support Equipment (EGSE) for optical scientific payload.

The space center of Liège carries out electronics and software involving techniques such as:

- Electrical cabinet design and manufacturing.
- Cable assembly design and manufacturing.
- PLC programming.
- Local and remote Human-Machine Interfaces (HMI) and Machine-to-Machine (M2M) under Windows or Linux.
- Exotic protocols with the equipment or with the customers.
- Thermal regulation.
- Data acquisition, logging, analysis and reporting.
- Actuation of mechanisms and valves.

[5]Nicolas Martin is the Head of Electronics lab.

- Fine positioning and compensation of optical elements and lasers.
- Control of digital cameras.
- Analog front-end electronics design and manufacturing.
- Scripting.

CSL works in close collaboration with :

- **FN HERSTAL** : develops, manufactures and sells a complete range of state-of-the-art, groundbreaking solutions developed around small caliber firearms and associated ammunition.
- **FZ** : technology and innovation leader specialized in the field of 70mm air-to-ground rocket systems (2.75 NATO Standard) in the defence market throughout the world.
- **AMOS** : delivers optical, mechanical and observation solutions using leading-edge technologies, for astronomy, space, science and industry.
- **DELTATEC** : high-level design house specialised in advanced technologies.

Furthermore, the electronics lab offers extensive design, prototyping, system engineering and project management services for the development of Instrument Control Units (ICU) and Remote Terminal Controllers (RTC) for optical scientific payloads for Space.

As part of the ULiege, they benefit from close partnership with the scientific community, particularly in the fields of:

- Observation of the Sun in the UV and EUV spectra
- Observation of the Earth in the visible spectrum
- X-ray detection
- Photometry

They also benefit from on-site environmental test facilities providing easy-access to vacuum thermal cycling, vibration, shock and specific optical calibration and verification equipment.

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